# Yokogawa AAI841-H00 S1

Installation, Diagnostics and Acceptance

## Work scope

Keep measurement and command assignments aligned while evaluating field references and receiver compliance separately. A paired transmitter/receiver circuit uses the eight-by-eight mapping and its recorded common references. The 310 mA at 5 V and 500 mA at 24 V maximum module demands belong in the node budget, independently of the receiving load.

**8 non-isolated current inputs** → **FIO shared-reference I/O** → **8 current-output receivers**

## 01 Before You Order

| Evidence to provide | Exact-model selection decision |
|---|---|
| **Current-input identity** | Request AAI841-H00 S1 and distinguish it from the AAB841 voltage-input execution; the similar mixed-I/O description does not establish the same input circuit. |
| **Eight-by-eight field drawing** | Provide input/output direction labels and shared reference connections for all sixteen signal circuits. |
| **Terminal and transmitter settings** | Photograph the ATA4S/ATA4D or ATK4A termination and per-input two-wire/four-wire setting. |
| **Timing and receiver record** | Identify the required input settling, output settling and receiver loads; the two conversion directions have different published step responses. |

## 02 Eight-by-eight non-isolated topology

### Preserve the input/output split

Identify all eight current inputs and eight current outputs before moving the termination. A sixteen-channel count alone does not describe this mixed-I/O topology.

### Recover common references

Map input and output common connections according to the actual field drawing. Do not import the isolated AAI835 connection strategy into this non-isolated module.

### Check terminal allocation

Match the installed ATA4S/ATA4D or ATK4A arrangement and channel-to-device mapping. Keep input and output field tags distinct.

### Plan both electrical budgets

Inputs require transmitter voltage compliance; outputs require an acceptable receiver load. These are different calculations even when both circuits use 4–20 mA.

## 03 Asymmetric response testing

| Observed condition / stage | Action and acceptance interpretation |
|---|---|
| **Prove inputs** | Apply a controlled input current and compare the indicated engineering value after the applicable input response. Record the non-isolated reference used by the test source. |
| **Prove outputs** | Command a controlled output and measure actual loop current at the receiver. The published output step response is 40 ms, distinct from the 100 ms input response. |
| **Avoid a false timing comparison** | Do not treat unequal input/output settling as evidence of module failure without accounting for their different documented responses and external device dynamics. |
| **Test paired process signals** | Capture transmitter value, control calculation, output command and receiver feedback as separate observations. This locates errors that a single loop-current measurement cannot resolve. |

## 04 Bank-level diagnosis and handover

| Observed condition / stage | Action and acceptance interpretation |
|---|---|
| **Several circuits affected** | Inspect common-reference and supply connections before replacing multiple field devices. Shared wiring can influence more than one otherwise correctly converted signal. |
| **Output open detected** | Check the receiver loop and current against the documented threshold. Keep open-loop diagnosis separate from a normal low-end process value. |
| **Replacement boundary** | Retain the H00 S1 identity, termination option and mixed-I/O topology. Preserve the S1 style marking in the replacement check; a base-family label does not establish equivalent hardware style. |
| **Sixteen-circuit evidence** | Retain direction-labeled assignments, input conversion tests, output-current/load tests and response conditions. Do not infer an untested output from a passing input. |

## 05 Quantitative field checkpoints

| Check | Verified condition | Practical evidence |
|---|---|---|
| **Input settling** | 100 ms specified input step response | Test input conversion with the non-isolated reference and the recorded controller filtering. |

## 05 Quantitative field checkpoints — continued

| Check | Verified condition | Practical evidence |
|---|---|---|
| **Output settling** | 40 ms specified output step response | Measure actual output current under the receiving load; do not compare settling against the input path blindly. |
| **Supply reservation** | 310 mA at 5 V; 500 mA at 24 V, maxima | Keep node-power assessment separate from the output load budget. |

## 06 Terminal and field-circuit selection map

| Order option / circuit | Applicable legacy selection |
|---|---|
| **/A4S00 / /A4S10** | ATA4S-00 / ATA4S-10 simplex pressure-clamp selections |
| **/A4D00 / /A4D10** | ATA4D-00 / ATA4D-10 dual-redundant selections |
| **/K4A00** | ATK4A-00 MIL adapter |
| **Input transmitter power** | ≥14.8 V at 20 mA; ≤26.4 V at zero current, before field-wire loss |

## Bare-module supply boundary

The offered AAI841-H00 S1 identity has no terminal-adapter option appended. Recover the installed terminal identity from its own label before assigning one of these selections to the replacement job.

## Technical applicability

Legacy AAI841-H00/H03 electrical and suffix specifications apply to the offered AAI841-H00 S1. S1 is retained as the offered style marking; it does not establish compatibility with later H50/H53 styles.

## Technical basis

Yokogawa Analog I/O Modules (for FIO), GS 33M50F30-40E, 5th Edition

## Related product navigation

Compare the separate system, revision and interface requirements on each linked product page. These portfolio references do not establish interchangeability.

| | |
|---|---|
| Yokogawa AAI143-H03 S1 | Analog I/O portfolio: compare signal direction, isolation and style. |
| Yokogawa AAI135-S50 S3 | Analog I/O portfolio: compare signal direction, isolation and style. |
| Yokogawa ALR121-S51 S1 | CENTUM system reference: retain its own host and configuration boundary. |

## Engineering contact



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