General Electric IS200VAICH1DBC

Engineering Installation and Acceptance Guide

Installed work boundary

The conversion board also supervises feedback and redundant-channel disagreement; field and software tests must be separated when diagnosing it.

Two TBAI groups	VAIC conversion	Mark VI controller

01 Rack exchange planning

Decision / observation	Action and acceptance evidence
Identify both terminations	Read the generation of both attached TBAI boards. Document the H1D-to-H1C-or-later pairing and the field circuits served by each cable group.
Preserve conversion settings	Save the range, engineering scale, acquisition and filter choices for the analog channels. A hardware identity cannot reconstruct the machine conversion settings.
Identify output duties	Record each receiving loop and whether it needs 20 mA or the higher-current selection. Review total load with the matched termination rather than using a receiver label alone.

02 Conversion-path acceptance

Decision / observation	Action and acceptance evidence
Restore the cable groups	Reconnect the two terminal groups to their assigned processor interfaces. Confirm channel numbers against the saved controller mapping before applying test quantities.
Separate range from scale	Inject approved points within the selected current or voltage range. Compare terminal signal, raw interpretation and engineering value so a range mismatch is not hidden by a plausible display.
Check dynamic settings	Apply an authorized input transition on the intended channel and compare filtering and acquisition behavior. The faster provision belongs to inputs 1-4 and is not a universal channel assumption.

03 Quantitative acceptance context

Decision / observation	Action and acceptance evidence
Acquisition period	A 100 Hz normal acquisition rate corresponds to 10 ms per acquisition. The 200 Hz provision on inputs 1-4 corresponds to 5 ms; neither number alone specifies complete machine response time.

03 Quantitative acceptance context - continued

Decision / observation	Action and acceptance evidence
Input accuracy interpretation	A full-scale accuracy expression must be applied to the selected input range, not to the instantaneous displayed reading. Retain the actual configured span with the comparison.
ADC versus effective resolution	The 16-bit conversion and 14-bit effective-resolution descriptions serve different purposes. More converter bits do not remove transmitter, wiring or engineering-scale uncertainty.
Output proof	The 12-bit DAC and 0.5% output accuracy do not establish the total actuator error. Include receiving-load and wiring conditions when evaluating delivered current.

04 Converter and diagnostic acceptance

Decision / observation	Action and acceptance evidence
Electrical limit versus process limit	Retain the hardware-limit flag, current terminal signal and configured high/low system limits. State which condition removed the input from scan and which condition only generated an application alarm.
Reset class record	After the actual cause is cleared, record the use and outcome of RESET_DIA or RESET_SYS as applicable. Do not substitute a global reset for identifying the original channel condition.
Redundant drift evidence	Retain individual rack values and voted median at the same test point. A stable overall value can coexist with an early deviation fault in one VAIC path.

Technical basis

GE Mark VI System Guide GEH-6421H, Volume I; GEH-6421M, Volume II

Related platform references - separate selection review

General Electric IS200TRTDH1CC	Resistance Temperature Detector Terminal Board
General Electric IS200VRTDH1DAC	RTD Input Processor Board

Engineering contact

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