A.6 CPU 1214C

A.6.1 General specifications and features

Table A-47 General

Technical data	CPU 1214C AC/DC/Relay	CPU 1214C DC/DC/Relay	CPU 1214C DC/DC/DC
Article number	6ES7214-1BG40-0XB0	6ES7214-1HG40-0XB0	6ES7214-1AG40-0XB0
Dimensions W x H x D (mm)	110 x 100 x 75		
Shipping weight	475 grams	435 grams	415 grams
Power dissipation	14 W	12 W	
Electrical current available (SM and CM bus)	1600 mA max. (5 V DC)		
Electrical current available (24 V DC)	400 mA max. (sensor power)		
Digital input current consumption (24 V DC)	4 mA/input used		

Table A-48 CPU features

Technical data		Description
User memory (Refer to "General technical specifications", (Page 1143) "Internal CPU memory retention".)	Work	150 Kbytes
	Load	4 Mbytes internal, expandable up to SD card size
	Retentive	14 Kbytes
Onboard digital I/O		14 inputs/10 outputs
Onboard analog I/O		2 inputs
Process image size		1024 bytes of inputs (I)/1024 bytes of outputs (Q)
Bit memory (M)		8192 bytes
Temporary (local) memory		• 16 Kbytes for startup and program cycle (including associated FBs and FCs) • 6 Kbytes for each of the other interrupt priority levels (including FBs and FCs)
Signal modules expansion		8 SMs max.
SB, CB, BB expansion		1 max.
Communication module expansion		3 CMs max.
High-speed counters		Up to 6 configured to use any built-in or SB inputs. Refer to "Hardware input pin assignment" (Page 526) for CPU 1214C: HSC default address assignments. • 100/[1]80 kHz (Ia.0 to Ia.5) • 30/[1]20 kHz (Ia.6 to Ib.5)
Pulse outputs[2]		Up to 4 configured to use any built-in or SB outputs • 100 kHz (Qa.0 to Qa.3) • 20 kHz (Qa.4 to Qb.1)

Technical data	Description
Pulse catch inputs	14
Time delay interrupts	4 total with 1 ms resolution
Cyclic interrupts	4 total with 1 ms resolution
Edge interrupts	12 rising and 12 falling (16 and 16 with optional signal board)
Memory card	SIMATIC memory card (optional)
Real time clock accuracy	+/- 60 seconds/month
Real time clock retention time	20 days typ./12 days min. at 40 °C (maintenance-free Super Capacitor)

[1] The slower speed is applicable when the HSC is configured for quadrature mode of operation.

[2] For CPU models with relay outputs, you must install a digital signal board (SB) to use the pulse outputs.

Table A-49 Performance

Type of instruction		Execution speed	
		Direct addressing (I, Q and M)	DB accesses
Boolean		0.08 µs/instruction	
Move	Move_Bool	0.3 µs/instruction	1.17 µs/instruction
	Move_Word	0.137 µs/instruction	1.0 µs/instruction
	Move_Real	0.72 µs/instruction	1.0 µs/instruction
Real Math	Add Real	1.48 µs/instruction	1.78 µs/instruction

Note

Many variables affect measured times. The above performance times are for the fastest instructions in this category and error-free programs.

A.6.2 Timers, counters and code blocks supported by CPU 1214C

Table A-50 Blocks, timers and counters supported by CPU 1214C

Element		Description
Blocks	Type	OB, FB, FC, DB
	Size	OB, FB, FC: 64 Kbytes DB: up to the size of work memory
	Address range for FBs, FCs, and DBs	FB and FC: 1 to 65535 (such as FB 1 to FB 65535) DB: 1 to 59999
	Nesting depth	16 from the program cycle or startup OB 6 from any interrupt event OB[1]
	Monitoring	Status of 2 code blocks can be monitored simultaneously

Element		Description
OBs	Program cycle	Multiple
	Startup	Multiple
	Time-delay interrupts	4 (1 per event)
	Cyclic interrupts	4 (1 per event)
	Hardware interrupts	50 (1 per event)
	Time error interrupts	1
	Diagnostic error interrupts	1
	Pull or plug of modules	1
	Rack or station failure	1
	Time of day	Multiple
	Status	1
	Update	1
	Profile	1
	MC-Interpolator	1
	MC-Servo	1
	MC-PreServo	1
	MC-PostServo	1
Timers	Type	IEC
	Quantity	Limited only by memory size
	Storage	Structure in DB, 16 bytes per timer
Counters	Type	IEC
	Quantity	Limited only by memory size
	Storage	Structure in DB, size dependent upon count type • SInt, USInt: 3 bytes • Int, UInt: 6 bytes • DInt, UDInt: 12 bytes

[1] Safety programs use two nesting levels. The user program therefore has a nesting depth of four in safety programs.

Table A-51 Communication

Technical data	Description
Number of ports	1
Type	Ethernet
HMI device	4
Programming device (PG)	1
Connections	• 8 connections for Open User Communication (active or passive): TSEND_C, TRCV_C, TCON, TDISCON, TSEND, and TRCV • 8 CPU-to-CPU connections (client or server) for GET/PUT data • 6 connections for dynamic allocation to either GET/PUT or Open User Communication • 64 connections for security certificates max.
Data rates	10/100 Mb/s
Isolation (external signal to logic)	Transformer isolated, 1500 V AC (type test)[1]

Technical data	Description
Cable type	CAT5e shielded
Interfaces	
Number of PROFINET interfaces	1
Number of interfaces PROFIBUS	0
Interface	
Interface Hardware	
Number of ports	1
Integrated switch	No
RJ-45 (Ethernet)	Yes; X1
Protocols	
PROFINET IO controller	Yes
PROFINET IO device	Yes
SIMATIC communication	Yes
Open IE communication	Yes
Web server	Yes
Media redundancy	No
PROFINET IO controller	
Services	
PG/OP communication	Yes
S7 routing	Yes
Isochronous mode	No
Open IE communication	Yes
IRT	No
MRP	No
PROFIenergy	Yes. The S7-1200 CPU only supports the PROFIenergy entity (with I-device functionality).
Prioritized startup	Yes (max. 16 PROFINET devices)
Number of connectable I/O devices max.	16
Number of IO devices that you can connect for RT, max.	16
Of which are in line, max.	16
Number of IO devices that can be activated/ deactivated simultaneously, max.	8
Update times	The minimum value of the update time also depends on the communication component set for PROFINET IO, on the number of IO devices, and the quantity of configured user data.
With RT	
Send clock of 1 ms	1 ms to 512 ms
PROFINET IO device	
Services	
PG/OP communication	Yes
S7 routing	Yes
Isochronous mode	No
Open IE communication	Yes

Technical data		Description
IRT, supported		No
MRP, supported		No
PROFIenergy		Yes
Shared device		Yes
Number of IO controllers with shared device, max.		2
SIMATIC communication		
S7 communication, as server		Yes
S7 communication, as client		Yes
User data per job, max.		See online help (S7 communication, user data size)
Open IE communication		
TCP/IP:		Yes
	Data length, max.	8 KB
	Several passive connections per port, supported	Yes
ISO-on-TCP (RFC1006):		Yes
	Data length, max.	8 KB
UDP		Yes
	Data length, max.	1472 bytes
DHCP		No
SNMP		Yes
DCP		Yes
LLDP		Yes

[1] Ethernet port isolation is designed to limit hazard during short term network faults to hazardous voltages. It does not conform to safety requirements for routine AC line voltage isolation.

Table A-52 Power supply

Technical data		CPU 1214C AC/DC/Relay	CPU 1214C DC/DC/Relay	CPU 1214C DC/DC/DC
Voltage range		85 to 264 V AC	20.4 V DC to 28.8 V DC	
Line frequency		47 to 63 Hz	--	
Input current (max. load)	CPU only	100 mA at 120 V AC 50 mA at 240 V AC	500 mA at 24 V DC	
	CPU with all expansion accessories	300 mA at 120 V AC 150 mA at 240 V AC	1500 mA at 24 V DC	
Inrush current (max.)		20 A at 264 V AC	12 A at 28.8 V DC	
I^2t		0.8 A^2 s	0.5 A^2 s	
Isolation (input power to logic)		1500 V AC	Not isolated	
Ground leakage, AC line to functional earth		0.5 mA max.	-	
Hold up time (loss of power)		20 ms at 120 V AC 80 ms at 240 V AC	10 ms at 24 V DC	
Internal fuse, not user replaceable		3 A, 250 V, slow blow		

Table A-53 Sensor power

Technical data	CPU 1214C AC/DC/Relay	CPU 1214C DC/DC/Relay	CPU 1214C DC/DC/DC
Voltage range	20.4 to 28.8 V DC	L+ minus 4 V DC min.	
Output current rating (max.)	400 mA (short-circuit protected)		
Maximum ripple noise (<10 MHz)	< 1 V peak to peak	Same as input line	
Isolation (CPU logic to sensor power)	Not isolated		

A.6.3 Digital inputs and outputs

Table A-54 Digital inputs

Technical data	CPU 1214C AC/DC/Relay	CPU 1214C DC/DC/Relay	CPU 1214C DC/DC/DC
Number of inputs	14		
Type	Sink/Source (IEC Type 1 sink)		
Rated voltage	24 V DC at 4 mA, nominal		
Continuous permissible voltage	30 V DC, max.		
Surge voltage	35 V DC for 0.5 sec.		
Logic 1 signal (min.)	15 V DC at 2.5 mA		
Logic 0 signal (max.)	5 V DC at 1 mA		
Isolation (field side to logic)	707 V DC (type test)		
Isolation groups	1		
Filter times	us settings: 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0 ms settings: 0.05, 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0		
HSC clock input rates (max.) (Logic 1 Level = 15 to 26 V DC)	100/80 kHz (Ia.0 to Ia.5) 30/20 kHz (Ia.6 to Ib.5		
Number of inputs on simultaneously	• 7 (no adjacent points) at 60 °C horizontal or 50 °C vertical • 14 at 55 °C horizontal or 45 °C vertical		
Cable length (meters)	500 m shielded, 300 m unshielded, 50 m shielded for HSC inputs		

Table A-55 Digital outputs

Technical data	CPU 1214C AC/DC/Relay and DC/DC/Relay	CPU 1214C DC/DC/DC
Number of outputs	10	
Type	Relay, mechanical	Solid state - MOSFET (sourcing)
Voltage range	5 to 30 V DC or 5 to 250 V AC	20.4 to 28.8 V DC
Logic 1 signal at max. current	--	20 V DC min.
Logic 0 signal with 10 KΩ load	--	0.1 V DC max.
Current (max.)	2.0 A	0.5 A
Lamp load	30 W DC / 200 W AC	5 W
ON state resistance	0.2 Ω max. when new	0.6 Ω max.

Technical data	CPU 1214C AC/DC/Relay and DC/DC/Relay	CPU 1214C DC/DC/DC
Leakage current per point	--	10 µA max.
Surge current	7 A with contacts closed	8 A for 100 ms max.
Overload protection	No	
Isolation (field side to logic)	1500 V AC (coil to contact) None (coil to logic)	707 V DC (type test)
Isolation groups	2	1
Isolation (group-to-group)	1500 V AC[1]	--
Inductive clamp voltage	--	L+ minus 48 V DC, 1 W dissipation
Switching delay (Qa.0 to Qa.3)	10 ms max.	1.0 µs max., off to on 3.0 µs max., on to off
Switching delay (Qa.4 to Qb.1)	10 ms max.	5 µs max., off to on 20 µs max., on to off
Maximum relay switching frequency	1 Hz	--
Pulse Train Output rate	Not recommended [2]	100 kHz (Qa.0 to Qa.3)[3], 2 Hz min. 20 kHz (Qa.4 to Qb.1)[3]
Lifetime mechanical (no load)	10,000,000 open/close cycles	--
Lifetime contacts at rated load	100,000 open/close cycles	--
Behavior on RUN to STOP	Last value or substitute value (default value 0)	
Control of a digital input	Yes	
Parallel outputs for redundant load control	Yes (with same common)	
Parallel outputs for increased load	No	
Number of outputs on simultaneously	• 5 (no adjacent points) at 60 °C horizontal or 50 °C vertical • 10 at 55 °C horizontal or 45 °C vertical	
Cable length (meters)	500 m shielded, 150 m unshielded	

1 Relay group-to-group isolation separates line voltage from SELV/PELV and separates different phases up to 250 V AC line to ground.

2 For CPU models with relay outputs, you must install a digital signal board (SB) to use the pulse outputs.

3 Depending on your pulse receiver and cable, an additional load resistor (at least 10% of rated current) may improve pulse signal quality and noise immunity.

A.6.4 Analog inputs

Table A-56 Analog inputs

Technical data	Description
Number of inputs	2
Type	Voltage (single-ended)
Full-scale range	0 to 10 V
Full-scale range (data word)	0 to 27648
Overshoot range	10.001 to 11.759 V

Technical data	Description
Overshoot range (data word)	27649 to 32511
Overflow range	11.760 to 11.852 V
Overflow range (data word)	32512 to 32767
Resolution	10 bits
Maximum withstand voltage	35 V DC
Smoothing	None, Weak, Medium, or Strong See the table for Step response (ms) for the analog inputs of the CPU (Page 1184).
Noise rejection	10, 50, or 60 Hz
Impedance	≥100 KΩ
Isolation (field side to logic)	None
Accuracy (25 °C / -20 to 60 °C)	3.0% / 3.5% of full-scale
Cable length (meters)	100 m, shielded twisted pair

A.6.4.1 Step response of the built-in analog inputs of the CPU

Table A-57 Step Response (ms), 0 V to 10 V measured at 95%

Smoothing selection (sample averaging)	Rejection frequency (Integration time)		
	60 Hz	**50 Hz**	**10 Hz**
None (1 cycle): No averaging	50 ms	50 ms	100 ms
Weak (4 cycles): 4 samples	60ms	70 ms	200 ms
Medium (16 cycles): 16 samples	200 ms	240 ms	1150 ms
Strong (32 cycles): 32 samples	400 ms	480 ms	2300 ms
Sample time	**4.17 ms**	**5 ms**	**25 ms**

A.6.4.2 Sample time for the built-in analog ports of the CPU

Table A-58 Sample time for built-in analog inputs of the CPU

Rejection frequency (Integration time selection)	Sample time
60 Hz (16.6 ms)	4.17 ms
50 Hz (20 ms)	5 ms
10 Hz (100 ms)	25 ms

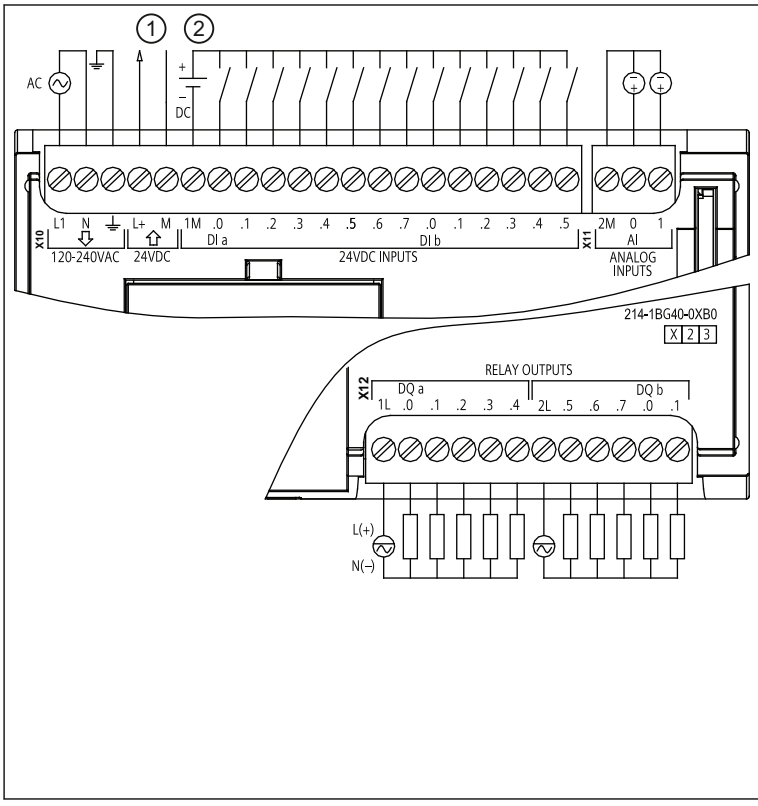
A.6.4.3 Measurement ranges of the analog inputs for voltage (CPUs)

Table A-59 Analog input representation for voltage (CPUs)

System		Voltage Measuring Range	
Decimal	**Hexadecimal**	**0 to 10 V**	
32767	7FFF	11.852 V	Overflow
32512	7F00		
32511	7EFF	11.759 V	Overshoot range
27649	6C01		
27648	6C00	10 V	Rated range
20736	5100	7.5 V	
34	22	12 mV	
0	0	0 V	
Negative values		Negative values are not supported	

A.6.5 CPU 1214C wiring diagrams

Table A-60 CPU 1214C AC/DC/Relay (6ES7214-1BG40-0XB0)

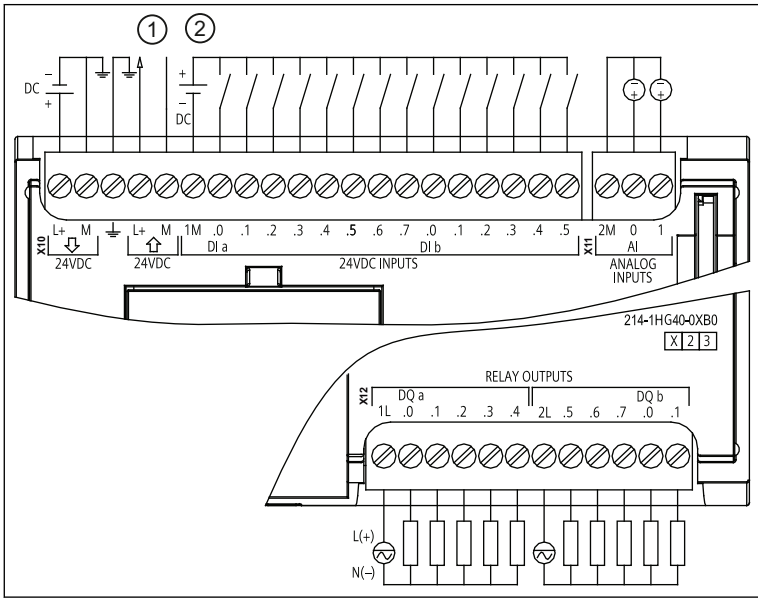


1	24 V DC Sensor Power Out For additional noise immunity, connect "M" to chassis ground even if not using sensor supply.
2	For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".
Note 1: X11 connectors must be gold. See Appendix C, Spare Parts for article number.	
Note 2: Either the L1 or N (L2) terminal can be connected to a voltage source up to 240 V AC. The N terminal can be considered L2 and is not required to be grounded. No polarization is required for L1 and N (L2) terminals.	
Note 3: See Device Configuratio (Page 121)n for information about the Ethernet port of the CPU.	

Table A-61 Connector pin locations for CPU 1214C AC/DC/Relay (6ES7214-1BG40-0XB0)

Pin	X10	X11 (gold)	X12
1	L1 / 120-240 V AC	2 M	1L
2	N / 120-240 V AC	AI 0	DQ a.0
3	Functional Earth	AI 1	DQ a.1
4	L+ / 24 V DC Sensor Out	--	DQ a.2
5	M / 24 V DC Sensor Out	--	DQ a.3
6	1M	--	DQ a.4
7	DI a.0	--	2L
8	DI a.1	--	DQ a.5
9	DI a.2	--	DQ a.6
10	DI a.3	--	DQ a.7
11	DI a.4	--	DQ b.0
12	DI a.5	--	DQ b.1
13	DI a.6	--	--
14	DI a.7	--	--
15	DI b.0	--	--
16	DI b.1	--	--
17	DI b.2	--	--
18	DI b.3	--	--
19	DI b.4	--	--
20	DI b.5	--	--

Table A-62 CPU 1214C DC/DC/Relay (6ES7214-1HG40-0XB0)



①	24 V DC Sensor Power Out For additional noise immunity, connect "M" to chassis ground even if not using sensor supply.
②	For sinking inputs, connect "-" to "M" (shown). For sourcing inputs, connect "+" to "M".
Note 1: X11 connectors must be gold. See Appendix C, Spare Parts for article number.	
Note 2: See Device Configuration (Page 121) for information about the Ethernet port of the CPU.	