Siemens 6ES7131-4BF00-0AA0

01 Map the eight field signals

1 Map the eight field signals
2 Restore the terminal assignment
3 Measure active and inactive states
4 Test the input-to-program path
5 Restore interlock ownership

Work sequence

Label each sensor or contact with its assigned DI number and controller bit. Record sensor supply distribution and any application substitution before isolating the field circuits.

Acceptance condition

The retained map resolves terminal position, channel and process function.

Digital inputs	8
Rated supply	24 V DC

Interleaved terminal order: Verify DI0–DI7 against the actual terminal numbering and controller byte mapping.

Record the observed condition, test method and result for this stage. Resolve any difference before moving to restore the terminal assignment.

Siemens 6ES7131-4BF00-0AA0

02 Restore the terminal assignment

1 Map the eight field signals

2 **Restore the terminal assignment**

3 Measure active and inactive states

4 Test the input-to-program path

5 Restore interlock ownership

Work sequence

Wire according to the interleaved DI terminal arrangement. Inspect the selected terminal base and provide the necessary sensor-supply distribution without confusing AUX and input terminals.

Acceptance condition

Each conductor reaches its intended input and supply reference.

Parameter length	3 bytes
Logic 1 range	15–30 V

Off-state acceptance: Two-wire leakage and the resulting input voltage must permit a reliable zero state.

Record the observed condition, test method and result for this stage. Resolve any difference before moving to measure active and inactive states.

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03 Measure active and inactive states

1 Map the eight field signals

2 Restore the terminal assignment

3 **Measure active and inactive states**

4 Test the input-to-program path

5 Restore interlock ownership

Work sequence

Check both voltage states with the actual sensor connected. For two-wire sensors, review leakage and confirm a reliable inactive state. Inspect shared reference and shielding where disturbances are present.

Acceptance condition

All inputs meet their intended logic state under actual field conditions.

Input current at logic 1	5 mA typical
Input delay	3 ms typical; 2–4.5 ms

Diagnostics boundary: Channel LEDs are state indicators; this module does not provide wire-break diagnostic functions.

Record the observed condition, test method and result for this stage. Resolve any difference before moving to test the input-to-program path.

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04 Test the input-to-program path

1 Map the eight field signals

2 Restore the terminal assignment

3 Measure active and inactive states

4 **Test the input-to-program path**

5 Restore interlock ownership

Work sequence

Operate each signal under controlled conditions and compare LED, raw input byte and application response. Include timing checks when pulse duration or synchronous acquisition matters.

Acceptance condition

The correct bit and process function respond without cross-assignment.

Cable length, unshielded	600 m maximum
Cable length, shielded	1000 m maximum

Interleaved terminal order: Verify DI0–DI7 against the actual terminal numbering and controller byte mapping.

Record the observed condition, test method and result for this stage. Resolve any difference before moving to restore interlock ownership.

Siemens 6ES7131-4BF00-0AA0

05 Restore interlock ownership

1. Map the eight field signals
2. Restore the terminal assignment
3. Measure active and inactive states
4. Test the input-to-program path
5. **Restore interlock ownership**

Work sequence

Remove temporary forces or substitutions and test the required process permissives. Retain final channel mapping and any timing or leakage findings.

Acceptance condition

Normal application logic owns every restored input.

Terminal 1 / 5	DI0 / DI1
Terminal 2 / 6	DI2 / DI3

Siemens 6ES7521-1BL00-0AB0

Siemens 6ES7331-7PF01-0AB0

Siemens 6ES7522-1BL01-0AB0

Related products require separate compatibility assessment. Retain the final configuration and signed test outcome.