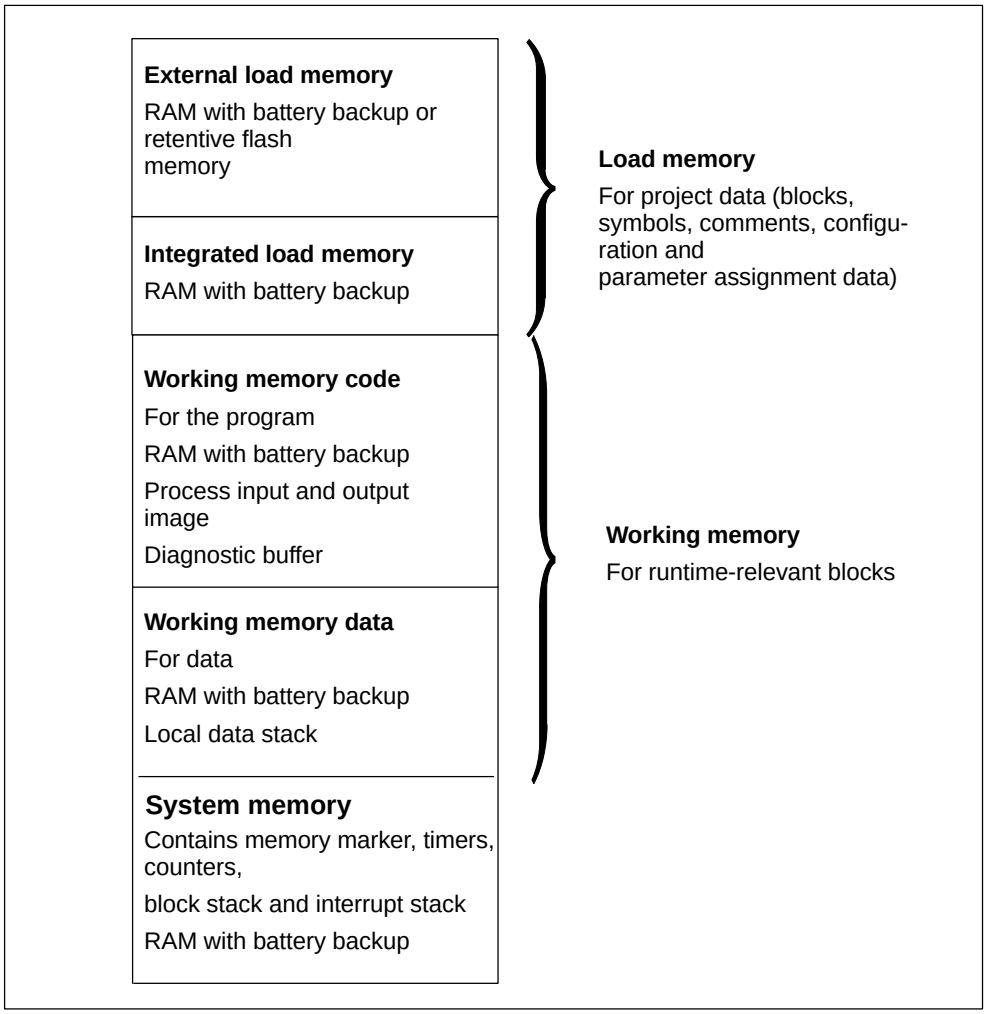
2.1 Overview of the Memory Concept of S7-400 CPUs

Subdivision of the Memory Areas

You can divide the memory of the S7 CPUs into the following areas:



Important Note for CPUs with Configurable Division of the Working Memory

If you use parameter assignment to change the division of the working memory, the working memory is reorganized when the system data are downloaded to the CPU. The result of this is that data blocks that were created with SFC are deleted, and the remaining data blocks are assigned initial values from the load memory.

The usable size of the working memory for code or data blocks is changed if you change the following parameters for loading the system data:

- Size of the process image (byte by byte; “Cycle/Clock Memory” tab)
- Communication resources (S7-400 only; “Memory” tab)
- Size of the diagnostic buffer (“Diagnostics/Clock” tab)
- Number of local data for all priority classes (“Memory” tab)

Basis for Calculating the Required Working Memory

To ensure that you do not exceed the available amount of working memory in the CPU, you must take into consideration the following memory requirements when assigning parameters:

Table 2-1 Memory Requirements

Parameter	Required Working Memory	In Code/Data Memory
Size of the process image (inputs)	12 bytes per byte in the process input image	Code memory
Size of the process image (outputs)	12 bytes per byte in the process output image	Code memory
Communication resources (communication jobs)	72 bytes per communication job	Code memory
Size of diagnostic buffer	20 bytes per entry in the diagnostic buffer	Code memory
Volume of local data	1 byte per byte of local data	Data memory

Memory Types in S7-400 CPUs

- Load memory for project data, such as blocks, configuration and parameter assignment data, including symbols and comments as of version 5.1.
- Working memory for the runtime-relevant blocks (code blocks and data blocks).
- System memory (RAM) contains the memory elements that each CPU makes available to the user program, such as memory markers, timers, and counters. The system memory also receives the block stack and the interrupt stack.
- System memory of the CPU also makes temporary memory available (local data stack, diagnostic buffer and communication resources) that is assigned to the program when a block is called for its temporary data. These data are only valid as long as the block is active.

  By changing the default values for the process image, local data, diagnostic buffer and communication resources (see the object properties of the CPU in HWCONFIG), you can control the working memory available to the runtime-relevant blocks.

Notice

Please note the following if you enlarge the process image of a CPU. Make sure that you configure the modules that can only be operated above the process image in such a way that they are also positioned above the enlarged process image. This particularly applies to IP and WF modules that you operate in the S5 adapter casing in a S7 400.

Flexible Memory Capacity

- Working memory:

  The capacity of the working memory is determined by selecting the appropriate CPU from the finely graded range of CPUs.

  In the case of the CPU 417, working memory can be expanded.
- Load memory:

  The integrated load memory is sufficient for small and medium-sized programs.

  The load memory can be increased for larger programs by inserting the RAM memory card.

  Flash memory cards are also available to ensure that programs are retained in the event of a power failure even if there isn't a backup battery. Flash memory cards can also be used (as of 2 MB for standard CPUs, as of 4 MB for fault-tolerant CPUs) to send and execute operating system updates.

Backup

- The backup battery provides backup power for the integrated and external part of the load memory, the data section of the working memory and the code section.

4.5 Technical Specifications of the CPU 416-2; (6ES7416-2XK02-0AB0, 6ES7416-2FK02-0AB0)

CPU and Version	
MLFB	6ES7416-2XK02-0AB0
• Firmware version	V 3.1
Associated programming package	As of STEP7 V 5.2
Memory	
Working memory	
• Integrated	0.8 Mbytes for code 0.8 Mbytes for data
• Expandable	No
Load memory	
• Integrated	256 Kbytes RAM
• Expandable FEPROM	With memory card (FLASH) up to 64 Mbytes
• Expandable RAM	With memory card (RAM) up to 64 Mbytes
Backup	Yes
• With battery	All data
• Without battery	None
Processing Times	
Processing times for	
• Bit operations	Min. 0.08 µs
• Word instructions	Min. 0.08 µs
• Integer math instructions	Min. 0.08 µs
• Floating-point math instructions	Min. 0.48 µs
Timers/Counters and Their Retentivity	
S7 counters	512
• Retentivity can be set	From Z 0 to Z 511
• Preset	From Z 0 to Z 7
• Counting range	1 to 999
IEC counter	Yes
• Type	SFB
S7 timers	512
• Retentivity can be set	From T 0 to T 511
• Preset	No retentive timers
• Time range	10 ms to 9990 s
IEC timers	Yes
• Type	SFB

Data Areas and Their Retentivity	
Total retentive data areas (including memory bits; times; counts)	Total working and load memory (with backup battery)
Memory markers	16 Kbytes
• Retentivity can be set	From MB 0 to MB 16383
• Preset retentivity	From MB 0 to MB 15
Clock memories	8 (1 memory byte)
Data blocks	Max. 4095 (DB 0 reserved)
• Size	Max. 64 Kbytes
Local data (can be set)	Max. 32 Kbytes
• Preset	16 Kbytes
Blocks	
OBs	See instruction list
• Size	Max. 64 Kbytes
Nesting depth	
• Per priority class	24
• Additionally in an error OB	2
FBs	Max. 2048
• Size	Max. 64 Kbytes
FCs	Max. 2048
• Size	Max. 64 Kbytes
Address Areas (Inputs/Outputs)	
Total I/O address area	16 Kbytes/16 Kbytes
• Of which distributed	
MPI/DP interface	2 Kbytes/2 Kbytes
DP interface	8 Kbytes/8 Kbytes
The distributed I/O address area is halved for each strand operated clock synchronously, i.e. in which an OB 61/62 is assigned.	
Process Image	16 Kbytes/16 Kbytes (can be set)
• Preset	512 bytes/512 bytes
• Number of partial process images	Max. 8
• Consistent data	Max. 244 bytes
Digital channels	131072/131072
• Of which central	131072/131072
Analog channels	8192/8192
• Of which central	8192/8192

Configuration	
Central racks/expansion units	Max. 1/21
Multicomputing	Max. 4 CPUs (with UR1 or UR2)
Number of plug-in IMs (overall)	Max. 6
• IM 460	Max. 6
• IM 463-2	Max. 4
Number of DP masters	
• Integrated	2
• Via IM 467	Max. 4
• Via CP	Max. 10
IM 467 cannot be used with the CP 443-5 Extended	
Number of plug-in S5 modules via adapter casing (in the central rack)	Max. 6
Operable function modules and communication processors	
• FM	Limited by the number of slots and the number of connections
• CP 440	Limited by the number of slots
• CP 441	Limited by the number of connections
• Profibus and Ethernet CPs incl. CP 443-5 Extended and IM 467	Max. 14

Time	
Clock	Yes
• Buffered	Yes
• Resolution	1 ms
• Accuracy at	
– Power off	Deviation per day 1.7 s
– Power on	Deviation per day 8.6 s
Runtime meter	8
• Number	0 to 7
• Value Range	0 to 32767 hours
• Granularity	1 hour
• Retentive	Yes
Time synchronization	Yes
• In PLC, on MPI and DP	as master or slave
Time of day difference in the system for synchronization via	
• ETHERNET	maximum 10 ms
• MPI	maximum 200 ms

S7 Message Functions	
Number of stations that can log on for message functions (e.g. WIN CC or SIMATIC OP)	Max. 12
Symbol-related messages	Yes
• Number of messages	
– Overall	Max. 1024
– 100 ms grid	Max. 128
– 500 ms grid	Max. 512
– 1000 ms grid	Max. 1024
• Number of additional values per message	
– With 100 ms grid	Max. 1
– With 500, 1000 ms grid	Max. 10
Block-related messages	Yes
• Simultaneously active ALARM-S/SQ blocks and ALARM-D/DQ blocks	Max. 200
ALARM-8 blocks	Yes
• Number of communication jobs for ALARM-8 blocks **and** blocks for S7 communication (can be set)	Max. 1800
• Preset	600
Process control reports	Yes
Number of archives that can log on simultaneously (SFB 37 AR_SEND)	32

Test and Startup Functions	
Monitor/modify variable	Yes
• Variables	Inputs/outputs, memory markers, DB, distributed inputs/outputs, timers, counters
• Number of variables	Max. 70
Force	Yes
• Variables	Inputs/outputs, memory markers, distributed inputs/outputs
• Number of variables	Max. 512
Status block	Yes
Single sequence	Yes
Diagnostic buffer	Yes
• Number of entries	Max. 3200 (can be set)
• Preset	120
Number of breakpoints	4

2nd Interface	
Type of interface	Integrated
Physical	RS 485/Profibus
Isolated	Yes
Power supply to interface (15 VDC to 30 VDC)	Max. 150 mA
Number of connection resources	32
Functionality	
• PROFIBUS DP	DP Master
DP Master	
• Utilities	
– Programming device/OP communication	Yes
– Routing	Yes
– Equidistance	Yes
– SYNC/FREEZE	Yes
– Enable/disable DP slaves	Yes
• Transmission rates	Up to 12 Mbps
• Number of DP slaves	Max. 125
• Address area	Max. 8 Kbytes inputs/ 8 Kbytes outputs
• User data per DP slave	In accordance with the DP slave, but a maximum of 128 bytes of inputs/128 bytes of outputs
DP slave	
As for the 1st interface	
Programming	
Programming language	LAD, FBD, STL, SCL
Instruction set	See instruction list
Bracket levels	8
System functions (SFC)	See instruction list
Number of SFCs active at the same time	
• WR_REC	8
• WR_PARM	8
• PARM_MOD	1
• WR_DPARM	2
• DPNRM_DG	8
• RDSYSST	1 to 8
• DP_TOPOL	1
System function blocks (SFB)	See instruction list
Number of SFBs active at the same time	
• RD_REC	8
• WR_REC	8
User program protection	Password protection
Access to consistent data in the process image	Yes
CiR synchronization time	
Base load	100 ms
Time per I/O byte	120 µs
Clock synchronism	
User data per clock synchronous slave	Max. 128 bytes
Maximum number of bytes and slaves in a process image partition	The following applies: Number of bytes / 50 + number of slaves < 26
Equidistance	Yes
Shortest clock pulse	5 ms 2.5 ms without use of SFC 126, 127
Dimensions	
Mounting dimensions W×H×D (mm)	25×290×219
Slots required	1
Weight	approx. 0.72 kg
Voltages, Currents	
Current consumption from S7-400 bus (5 VDC)	Typ. 1.5 A Max. 1.6 A
Current consumption from the S7-400 bus (24 VDC) The CPU does not consume any current at 24 V, and it only makes this voltage available at the MPI/DP interface.	Total current consumption of the components connected to the MPI/DP interfaces, with a maximum of 150 mA per interface
Backup current	Typ. 40 µA Max. 420 µA
maximum backup time	approx 356 days
Incoming supply of external backup voltage to the CPU	5 VDC to 15 VDC
Power loss	Typ. 7.5 W

CPU as DP Slave

You can only configure the CPU once as a DP slave even if the CPU has several interfaces.