Section 1.5
Detailed Specifications

Table 1-1. Thermocouple Temperature Ranges

Specification	Description			
Configuration	4/8 Channel of differential counter inputs 2/4 Channels of quadrature encoding 2/4 Input enable Control lines			
Input Modes	DC counter, AC flow meter			
Voltage Range	AC 0-30 VP	5 VDC	12 VDC	24 VDC
VIL	-50 mV	1 V	3 V	5 V
VIH	+50 mV	3.5 V	9 V	13 V
Vmax (CE)	±75 V	±75 V	±75 V	±75 V
Vmax (UL)	±100 V	±100 V	±100 V	±100 V
Current Range	5 mA maximum at 120 V			
Input Impedance	Rin greater than 10 ohms when within -10 V to +12 V range. Rin = 25 Kohms when outside of -10 V to +12 V range Cin 100 pF Input Filter Off Cin 1000 pF Input Filter On			
Counter Speed	DC Inputs 0 Hz to 50 kHz AC Inputs 0 Hz to 50 kHz			
Input Frequency	DC Inputs 1 Hz to 50 kHz AC Inputs 1 Hz to 50 kHz			
Counter Enable Input	VIL 1.0 V maximum VIH 3.5 V minimum Vmax 75 V			
Input impedance	25 Kohms			
Input Filter: Digital Filter Digital Filter Analog Filter	 50 kHz (Default) 30 kHz 15 kHz			
Min Pulse Time: DC mode External Enable/Disable	 8 us Enable and Disable setup time = 20 us			
Channel Update Time: Counter Output Rate Output: Rate Instantaneous Mode Rate Average Mode	 Scaling OFF ON 4.00 5.6 (msec per channel) 4.00 5.6 (msec per channel) 1.00 1.00 (sec per channel)			

Specification	Description	
Accuracy: Count mode Rate (Instant) Rate (Average)	 ± 1 Count ± 1% at 50 kHz, .001% at 1 Hz ± 1 Hz	
Maximum Count Value	Low Range -32,768 to +32,767 High Range -8,388,608 to +8,388,607	
Fault detection	Over and under range status bits, for all modes.	
Data Format: Counter mode Rate mode	 Max Binary Value: -8,388,608 to +8,388,607 Max Binary Value: -32,768 to +32,767	
Isolation: Channel to Rack Channel to Channel	 1000 VDC Continuous Optical and magnetic 0 VDC	
Input Protection	Maximum input voltage ±100 VDC, 150 VAC peak-to-peak Maximum input current ±5 mA at 100 VDC	
Power Requirements:	CTR4	CTR8
Internal rack +5 V	17 5mA	225 mA
Internal rack +24 V	75 mA	125 mA

Table 1-2 Physical Specifications

Specification	Description
LED Indicators	
Module Status	The Module Status LED indicates the status of the power up self-test. The LED is on when the module is ready. Any self -test error is indicated with a blink code.
Channel Status	CTR4 - 4 Green LEDs CTR8 - 8 Green LEDs The 8 Channel LEDs indicate that a channel is enabled.
Terminal Block	24-pin removable connector.
Wire Size	One 12 AWG to 28 AWG wire
Torque	0.5 Nm, (4.5 lb.-in)

Table 1-3 Environmental Specifications

Specification	Description
Operating Temperature	-0 ºC to 60 ºC (32 ºF to 140 ºF)
Storage/Non-Operating Temperature	-40 ºC to 85 ºC (-40 ºF to 185 ºF)
Operating Humidity	5% to 95%, non-condensing

Chapter 3
Configuring the 1746sc-CTR4/CTR8

This chapter explains how the module and the SLC processor communicate through the processor's I/O image tables. It also describes the module's input filter characteristics. Topics discussed include:

- Module ID code.
- Module addressing.
- Operating modes.
- Input configurations.
- Gate modes.
- Channel turn-on/turn-off/reconfiguration timing.
- Response to slot disabling.

Section 3.1
Module ID Code

The module ID code is a unique number assigned to each type of 1746 I/O module. The ID defines for the processor the type of I/O module and the number of words used in the processor's I/O image table. With APS software, use the system I/O configuration display to manually enter the module ID when assigning the slot number during the configuration. Do this by selecting (other) from the list of modules on the system I/O configuration display and enter 10200 as the ID code for the 1746sc-CTR4 and 10401 as the ID code for the 1746sc-CTR8.

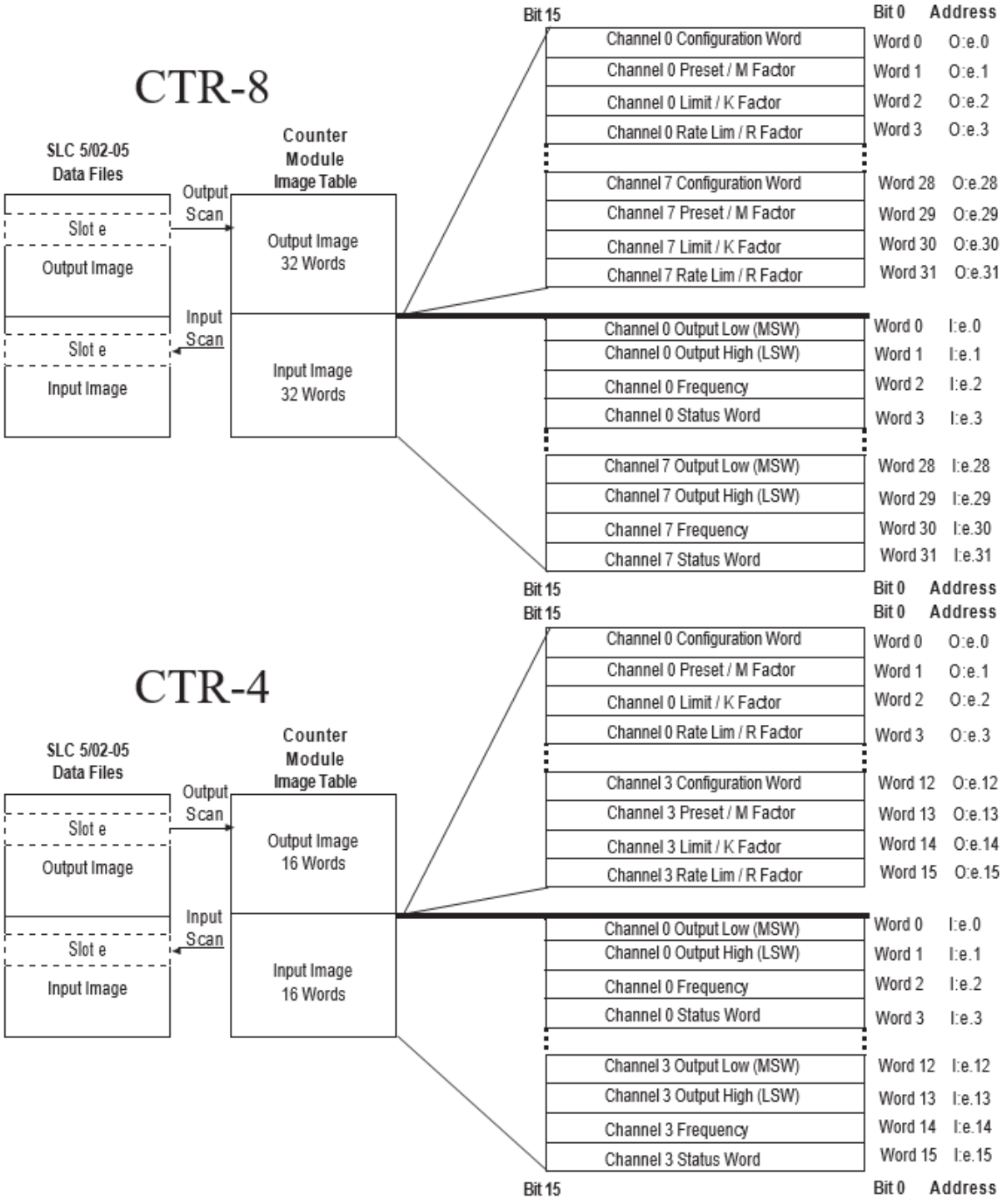
No special I/O configuration (SPIO CONFIG) is required. The module ID automatically assigns the correct number of input and output words.

If you are using different programming software package, refer to the documentation that came with your software.

Section 3.2
Module Addressing

The CTR-8 module uses 32 input and 32 output registers, and the CTR-4 module uses 16 input and 16 output registers. Both modules use Class III mode operation and cannot be used with Class I operation. The following memory map shows you how the SLC processor's output and input tables are defined for the module. The SLC 5/01 processor does not support Class III operation and is not compatible with this module. This module is not suitable for use in remote rack applications with ASB modules due to the input / output word size. The following memory map shows you how the SLC processor's output and input tables are defined for the module.

Figure 3-1. Image Table



Output Image - Configuration Words

Thirty-two (CTR-8) or sixteen (CTR-4) words of the SLC processor's output image table are reserved for the module. For the CTR8, output image words 0-31 are used to configure input channels 0-7. For the CTR4, output image words 0-15

Uni-Directional

With this configuration, the input increments in an upward direction. All 8 channels may be configured in the unidirectional mode. Every clock pulse will increment the counter on the rising edge.

NOTE	The direction of the counter may be inverted by setting the Count Direction bit described in the Configuration chapter.

Bi-Directional

The bidirectional counter requires 2 input channels. In this mode one channel is used as the counter input and the second channel is used to determine the count direction. The counter will increment when the Direction Channel value is 0 and will decrement when the Counter Direction Channel value is 1.

X1 Quadrature Encoder

The quadrature mode requires 2 input channels. When a quadrature encoder is attached to an input channel pair, A and B, the count direction is determined by the phase angle between inputs A and B. If A leads B, the counter increments. If B leads A, the counter decrements. (The counter changes value only on one edge of input 1.) The counter increments once per quadrature cycle.

NOTE	The X1 Quadrature mode provides additional Anti-Jitter circuitry. This distinguishes between a valid quadrature sequence and an invalid sequence due to electrical noise or jitter. Jitter can occur if a quadrature encoder stops rotating right at an input sensor trip point. This can cause additional unwanted clock pulses. The X1 quadrature mode can detect invalid transitions and filter these out.

X4 Quadrature Encoder

Like the X1 quadrature encoder, the count direction is determined by the phase angle between inputs A and B. If A leads B, the counter increments. If B leads A, the counter decrements. However, the counter changes value on the rising and falling edges of inputs A and B. The counter increments four times per quadrature cycle.

NOTE	The module's Channel LEDs only indicate the state of the counters start/stop bit. They do not indicate that state of the external hardware gate.

Counter Start / Stop Bit

This bit allows the counter to continue to count up or down from its present value. Starting, or enabling this bit will not override the external counter input.

Section 3.6 Channel Turn-On, Turn-Off, and Reconfiguration Times

The time required for the module to recognize a new configuration for a channel is one module update time.

- Turn-off time requires up to one module update time.
- Reconfiguration time is the same as turn-on time.

Section 3.7 Response to Slot Disabling

By writing to the status file in the modular SLC processor, you can disable any chassis slot. Refer to your SLC programming manual for the slot disable/enable procedure.

WARNING	**POSSIBLE EQUIPMENT OPERATION** Always understand the implications of disabling a module before using the slot disable feature. Failure to observe this precaution can cause unintended equipment operation which may cause injury to personnel or damage to equipment.

Input Response

When a counter slot is disabled, the counter module continues to update its input image table. However, the SLC processor does not read input from a module that is disabled. Therefore, when the processor disables the counter module slot, the module inputs appearing in the processor table is not read. When the processor re-enables the module slot, the current state of the module inputs is read by the processor during the subsequent scan.

Output response

The SLC processor may change the counter module output data (configuration) as it appears in the processor output image. However, this data is not transferred to the counter module. The outputs are held in their last state. When the slot is re-enabled, the data in the processor image is transferred to the counter module.