Emerson IC695ALG728

01 Analog and HART layers

The current loop and digital device conversation coexist. A valid analog command can remain present even when digital retries or pass-through traffic delay a device variable.

Current-loop and voltage-output configurations impose different load requirements. Establish the receiving interface and field-power arrangement before selecting a range or evaluating the suitability of a replacement output channel.

Output channels	8, non-isolated
Current output	0–20 mA or 4–20 mA

Technical basis: Emerson PACSystems RX3i System Manual, GFK-2314AG. This Apter Power technical reference organizes applicable manufacturer data.

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02 Voltage-mode receiving load

Use the minimum permitted resistance for voltage receivers and include any parallel measuring instrument. A lower combined resistance increases output loading beyond the intended operating condition.

Available loop voltage must cover the complete connected burden at the commanded current. Include the receiving input and cable loss in that assessment; a nominally correct supply alone does not establish compliance.

Voltage output	±10 V or 0–10 V
External supply	19.2–30 V DC; 250 mA maximum

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03 Current-loop headroom

Current regulation depends on supply headroom over the load voltage. Assess wiring and receiver burden at the minimum available supply, not only during a nominal bench test.

Analog command refresh and HART communication are distinct timing functions. Document which process decisions depend on the electrical output and which depend on device messages when defining the required response.

HART protocol	Version 5.0
Analog update	About 16 ms with HART; 8 ms without HART, all channels

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04 Release-dependent bus demand

Earlier and later module executions have different backplane-current maxima. Distinguish the electronics supply from the external field supply when checking cabinet power.

Output behavior during abnormal operation belongs in the application design. Record the configured fallback decision for each affected final element and verify it against the permitted process safe state.

Current load	850 Ω maximum at 20 V supply
Voltage load	2 kΩ minimum

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05 HART scheduling

Channels are organized into acquisition groups, and retries or additional variables affect digital update timing. Treat device-variable freshness as a separate condition from analog output refresh.

Thermal and supply limits apply to the assembled installation. Evaluate the number of simultaneously loaded outputs and the enclosure conditions rather than treating a single channel test as proof of full-module operation.

Settling to 95%	70 ms current with HART; 23 ms without HART; 2 ms voltage

Related product navigation

Emerson IC695ALG608

General Electric IC693CPU374 PLUS

These are related references, not confirmed substitutes or an automatically approved assembly.