NI PCI-6224

01 Multifunction PCI Data Acquisition Device / system role

Product function

Channel configuration and sampling distribution determine how the available conversion throughput is shared across the acquisition task.

Selected configuration

Differential acquisition improves measurement flexibility but does not remove the input common-mode boundary. Source impedance and channel-to-channel voltage steps affect settling; using the maximum aggregate sample rate does not guarantee the tightest accuracy for every multiplexed signal sequence.

Integration checkpoints

- Preserve acquisition tasks
- Check analog references
- Assign shared digital terminals
- Accept the complete measurement task

Acquisition architecture	shared conversion throughput across the configured scan
Signal integrity	manage settling and common-mode voltage
Timing resources	coordinate analog, digital and counter-driven tasks

Digital waveform operations use Port 0 and require a sample clock from another supported subsystem or an external source. Static digital lines and timing terminals have separate roles. The application must assign those resources and data transfers deliberately to avoid conflicts between simultaneous measurement tasks.

PCI-6224

02 Technical operating envelope

Analog inputs	32 single-ended or 16 differential
ADC resolution	16 bits
Maximum aggregate sampling	250 kS/s
Input ranges	±0.2 V; ±1 V; ±5 V; ±10 V
Maximum working voltage	±11 V relative to AI GND, signal plus common mode

Digital lines	48
Input FIFO	4095 samples
Timing accuracy	50 ppm of sample rate
Digital waveform port	Port 0, up to 32 lines

Values retain their individual conditions and interface boundaries. Technical values apply to PCI-6224 with the stated operating conditions. Check supplied revision and the configured installation.

Why is a full-scale step more demanding for PCI-6224 than repeated samples of one stable signal?

Multiplexer switching introduces a new voltage that must settle. The required conversion interval depends on the acceptable residual error and the source conditions.

Can PCI-6224 digital waveform generation run from its own independent timing engine?

The digital subsystem requires a supported clock from another device subsystem or an external source. Allocate that clock explicitly when designing a timed digital task.

PCI-6224

03 System integration and applications

Multiplexed laboratory acquisition

Distribute aggregate throughput among analog channels with suitable source impedance and settling time.

PC-based machine test

Combine analog measurements with digital status under a deliberately allocated timing configuration.

Triggered measurements

Use compatible trigger and PFI routing to align the acquisition task with the event of interest.

Synchronized digital tasks

Supply a supported digital sample clock and check resource sharing with other device functions.

System and supply context

The PCI-6224 belongs to the NI M Series PCI acquisition arrangement with its specified field interfaces.

Application boundary

Applications must satisfy the module or transducer boundary and the actual controller, receiver or target conditions.

Why can a high-impedance source reduce PCI-6224 multiplexed measurement accuracy?

After switching channels, the input must settle through the source impedance. Increase settling time or use an appropriate buffered source when large steps and high impedance cause errors.

PCI-6224

04 Engineering selection decisions

How does scanning more channels affect the per-channel rate of PCI-6224?

The maximum multichannel rate is aggregate. Divide the available scan throughput among the configured channels and allow the required conversion interval for settling.

Does differential mode protect PCI-6224 from excessive common-mode voltage?

No. Signal plus common-mode voltage must remain within the working limit relative to AI GND. Differential wiring does not provide galvanic isolation.

How should PCI-6224 PFI lines be assigned when digital I/O and triggers coexist?

Review each terminal’s selected function so a timing route does not conflict with a static digital assignment. The shared terminal cannot be treated as two independent pins.

What distinguishes an PCI-6224 FIFO problem from a signal-wiring problem?

A transfer overrun concerns host and buffer servicing, whereas a wrong or noisy value may arise in the analog circuit. Check acquisition status and data-transfer timing before altering field wiring.

PCI-6224

05 Configuration boundary and references

Lifecycle and support

PCI-6224 is in the Limited Support phase. New purchase is unavailable; repair, calibration and technical-support availability are limited and require confirmation for the individual service request.

Replacement assessment

Save channel modes, scan order, ranges, clocks and trigger routes. Record the PCI installation and connector assignments used by the application.

Document roles

Use the original manufacturer excerpt for its preserved technical tables and drawings. This product brief explains selection and system context. The separate installation guide covers preparation, connection, tests and handover; use it together with the applicable manufacturer instructions.

Technical basis

NI 6224 Device Specifications, 375202C-01.

Related product navigation

- Siemens 6ES7232-4HD32-0XB0
- Siemens 6ES7431-7QH00-0AB0

These are related references, not confirmed substitutes or an automatically approved assembly.

Product enquiries