VIPA 214-2BM02

01 CPU memory and DP process image

1 Retain the CPU 214 project

Back up the 48/80 KB CPU 214DPM application and hardware configuration. Check that a replacement project has not been built for a larger neighboring CPU.

2 Budget DP process data

Total the configured input and output bytes independently. Keep each direction within 1,024 bytes as well as respecting the slave-count limit.

Work memory	48 KB
Load memory	80 KB
DP input/output capacity	1,024 bytes each direction

214-2BM02

02 Segment population and cable reach

1 Count stations by segment

Record each repeater boundary and count the stations on every segment. Do not apply the overall 125-slave master limit to a single unrepeated cable segment.

2 Verify rate and cable length

Compare the selected transfer rate with the installed cable length. At 12 Mbit/s, retain the 100 m maximum for a segment without a repeater.

PROFIBUS rate	9.6 kbit/s to 12 Mbit/s
Segment length at 12 Mbit/s	100 m without repeater
Stations per segment	32 maximum without repeater

03 Bus endings and power connection

1 Inspect both bus ends

Check active termination at the two ends of each linear segment and the power needed by that termination. Avoid adding extra endpoint termination at intermediate devices.

2 Restore supply and connector seating

Confirm the 24 V input remains between 20.4 and 28.8 V. Seat the PROFIBUS D-sub and local module connections without changing the retained wiring order.

Supply voltage	24 V DC; 20.4–28.8 V permitted
Maximum current	1.5 A
Maximum power dissipation	5 W
PROFIBUS connector	9-pin D-sub

04 Master configuration and slave states

1 Load the correct hardware map

Restore the approved System 200V configuration and DP slave data assignments. Compare device addresses and I/O byte lengths with the retained project.

2 Check master and slave states

Observe PROFIBUS diagnostics and confirm data exchange with every expected slave. Investigate a missing station before enabling its dependent process outputs.

DP slaves	125 maximum
Fieldbus potential separation	≥500 V AC

214-2BM02

05 I/O mapping and network baseline

1 Verify application I/O mapping

Exercise representative inputs and outputs in a controlled state. Confirm that changes occur at the intended process addresses rather than only at the field device.

2 Save the segment baseline

Retain rate, cable length, repeater layout, termination, station count and I/O allocation. These values define the working DP installation for future service.

Technical basis: VIPA System 200V CPU Manual HB97E, revision 12/02.

Related product navigation

Siemens 6ES7216-2AD23-0XB8

Siemens 6ES7215-1BG40-0XB0

These are related references, not confirmed substitutes or an automatically approved assembly.