VIPA CPU-314SB-314-2AG13

01 CPU variant and memory allocation

Identify the 314-2AG13 hardware

Compare the installed CPU and its interface set with the 314SB/DPM order identity. Do not assume a SPEED-Bus connector from the SPEED7 processor name.

Retain memory and project configuration

Back up the application, data and hardware configuration. Record whether work-memory expansion is actually enabled before assessing replacement capacity.

Integrated load memory	512 KB
Standard work memory	256 KB
Maximum work memory	512 KB, supported expansion required
SPEED-Bus interface	Not fitted

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02 Supply conditions and interface role

Check the 24 V input

Verify polarity and the 20.4–28.8 V supply range, including startup behavior. Allow for the specified inrush rather than sizing the circuit only from idle consumption.

Restore the selected interface role

Confirm whether the integrated port is used as PROFIBUS master, slave or point-to-point. Restore the corresponding project and field wiring without mixing these operating roles.

Supply voltage	24 V DC; 20.4–28.8 V permitted
Rated current	1 A
Idle current	200 mA
Inrush current	5 A

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03 PROFIBUS addressing and termination

Review DP address allocation

Check the configured slave addresses and input/output data assignment against the retained project. The maximum slave count does not remove the per-device data limitations.

Restore the bus termination

Use the installed PROFIBUS cable and termination plan for the selected rate. Check both bus ends and avoid treating an intermediate station as an endpoint.

PROFIBUS rate	9.6 kbit/s to 12 Mbit/s
DP master slaves	124 maximum

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04 Application restoration and diagnostics

Load and compare the application

Transfer the approved program and hardware configuration, then compare the loaded state with the backup. Check retained data before enabling normal process outputs.

Interpret CPU and DP indications

Observe CPU state together with PROFIBUS run, error and data-exchange indicators. A CPU in RUN can still have a missing or incorrectly configured slave.

Minimum bit/word instruction	0.01 µs
Power loss	6 W

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05 Instruction timing and system baseline

Measure the actual scan behavior

Review task execution and communication under representative load. Do not substitute the minimum bit-instruction time for an application-cycle measurement.

Retain the restored configuration

Save memory allocation, interface role, slave map, diagnostics and the tested application state. Resolve bus or memory discrepancies before returning the controller to service.

Technical basis: VIPA System 300S CPU 314-2AG13, HB140, revision 14-40.

Related product navigation

Siemens 6ES7214-1BD23-0XB0

Siemens 6ES7216-2BD23-0XB0

These are related references, not confirmed substitutes or an automatically approved assembly.