Yokogawa ADV859-P00 S1

01 Document each isolated channel

1 Retain the ST2 wiring record

Identify the KS2 cable and record each input and output circuit. The 16 input and 16 output channels are individually isolated; keep their separate field references intact.

2 Confirm the offered execution

Check ADV859-P00 and the S1 style against the installed unit. Retain point names and output mode assignments before removing the module.

Channels	16 inputs; 16 outputs
Field interface	ST2 through KS2
Isolation	Individual channels

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02 Qualify input contacts

1 Inspect contact condition

Verify that the field contacts meet the 5 VDC / 20 mA minimum rating. Contamination or excessive contact resistance can prevent a dependable near-zero ON state.

2 Test both resistance states

Measure the full wiring path in its safe test condition. Closed resistance must be no greater than 200 Ω and open resistance at least 100 kΩ.

Contact ON	≤200 Ω
Contact OFF	≥100 kΩ
Voltage input ON	±1 VDC; source ≤200 Ω

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03 Reconnect the KS2 and loads

1 Preserve individual references

Reconnect the dedicated KS2 cable without introducing bridges between isolated channels. Compare terminal numbers with the retained ST2 circuit drawing.

2 Inspect output protection

Check each transistor load against 30 VDC and 100 mA. For a DC relay, retain the spark-killer diode and correct polarity.

Output construction	Transistor contact
Base current	Maximum 450 mA at 5 VDC
Load protection	Diode for DC relay

04 Verify distinct timing functions

1 Test a stable input state

Exercise input transitions and confirm the assigned point changes correctly. Treat the 8 ms module input response separately from complete application response time.

2 Check timed output modes

Use known pulse commands to verify the configured width or time proportion. The 8 ms resolution and additional ON/OFF delay must suit the actuator requirement.

Pulse width	8 ms–7200 s
Input response	8 ms
Output response	≤16 ms

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05 Return the ST2 interface to service

1 Resolve circuit disagreement

If a point fails, compare contact state, KS2 assignment, load protection and point mode. Do not correct a wiring fault by changing application logic without engineering review.

2 Retain isolated-channel evidence

Record the S1 marking, cable and terminal identities, contact thresholds and output tests. Confirm all affected circuits remain correctly separated after the test.

Technical basis: Yokogawa Digital I/O Modules (for FIO), GS 33J60F70-01EN, 5th edition.

Related product navigation

Yokogawa AAI835-S00 S2

Yokogawa AAI141-S00

These are related references, not confirmed substitutes or an automatically approved assembly.