1. Order number, Validity Definition

6DD 1601 - 0AE0 Processor board DC 16 MHz
for software version from 2.3

This documentation is only valid for the processor board PG16 with the SWE type number 4656019004.01 (type number is stamped on the product version plate).
The product version has to be > M.

Differences to the previous version :

- Analog output port to the SITOR interface
- Set-up possibilities for the long pulses and the external synchronization voltage starting from the software V 3.0
- Summated pulses at the X5 connector as a measurement signal for commissioning.

2. Functional Description

The processor board PG16 is designed in the SIMADYN D system for drive level control, numerical processing and regulating functions (torque shell) in the line commutated converters. The board incorporates a 16 bit 80C186-16 microprocessor with corresponding peripherals as well as the logic for generating the converter pulses.

The board can be programmed for both the user software and the system firmware (operating system, monitor program as well as the function module code) on plug in memory sub-modules (MSx) located in the X50 connector. The user code runs on the processor under the SIMADYN D real time operating system. This guarantees interrupt controlled cycle times, dependent upon the configuration, of≥ 1ms.

There are 4 binary inputs and 4 binary outputs available (Connector X6) for the fast exchange of data to a second PG (synchronization of two PG's). All four binary inputs can be declared as interrupt inputs by the software. The processor interrupts cyclic processing at the occurrence of an interrupt at one of these inputs and starts processing the interrupt function packet "Process Interrupt Job" (PIJ).

The serial interface (connector X01) is designed purely as a service interface. No communication can be configured via this interface. A dialog is only possible with the Hex monitor to the PG675/685 or televideo terminal and only with the corresponding hybrid board installed.

The seven segment display H1 on the board front plate shows the configured processor number in normal operation. The display flashes an error code, see /1/, when a fault occurs on the board.

The Hex monitor can be activated, when an error message is being displayed, by pressing the S1 key.

The double test jack X10 and X11 can be used to force a board reset (new start). This is implemented by jumpering the jacks with a switch or a shorting plug. The test jack X10 is also the ground connection for the test signals at X12-X15.

A 50 pin test connector X4 is available on the board for hardware diagnostics using a logic analyzer or a recorder. The recorder also requires a 10 pin connector X9 .

Three "watchdogs" are available for each processor board for monitoring the functionality of the hardware and software.

The hardware monitor checks:

- ready signal time outs during system bus accessing
- double address decoding errors
- whether addresses are accessed, that are not implemented
- system bus fault messages

The software monitor checks:

- whether the processor is still running a cyclic program
- whether the interrupt controller of the serial interfaces, timer and inputs are operating correctly.

A "Non Maskable Interrupt" (NMI) is generated when the watchdog detects a fault. The processor attempts to eliminate the fault and return to cyclic operation. If the fault is being caused by the processor, then it switches to an inactive state, activates the red dot on the seven segment display and the "system fault" line on the bus.

The processor board PG16 has a standard interface for controlling the SITOR thyristor sets. The corresponding signals are implemented on a 50 pin connector socket (X7).

The SITOR set provides the following signals for the processor board:

* synchronization voltage
* monitoring signals
* two signals for the detection of the rotating field direction
* current zero
* current actual value as proportional frequency value
* voltage actual value as proportional frequency value

The processor board PG16 supplies the trigger pulses for the thyristors of SITOR set for the torque direction I and torque direction II .

The diode pair H10 and H11 display which torque direction is currently active.

* LED H10 indicates the torque direction I.
* LED H11 indicates the torque direction II.

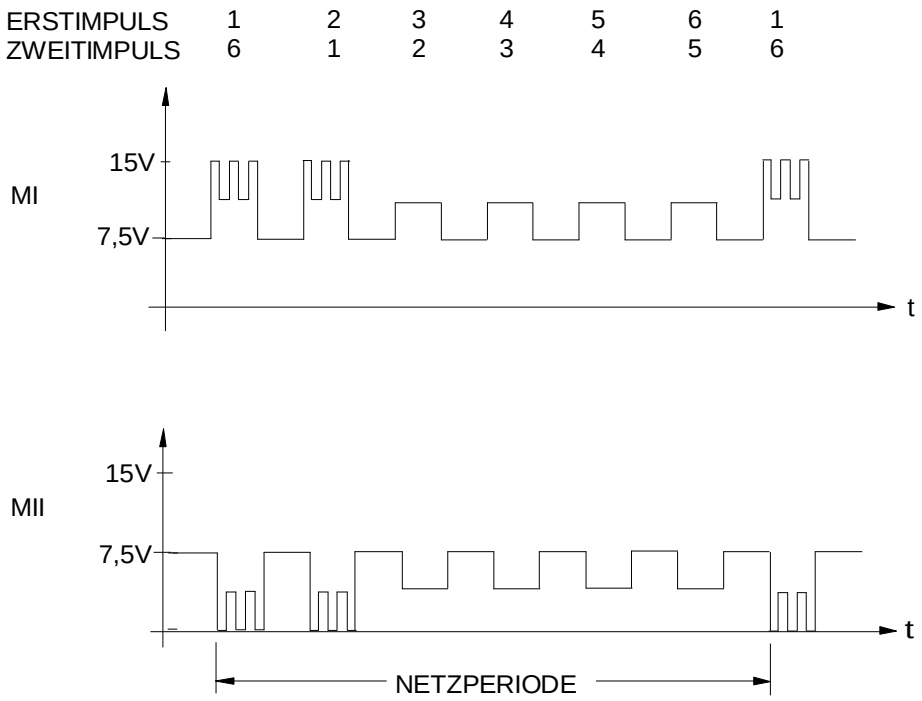
Two further double test jacks (X12-X15) are available on the PG16 for the output of converter specific measurement values. The reference or ground point is jack X10 :

* X12: phase to phase voltage L1-L3

* X13: analog current actual value for the connection of a conventional meter type instrument (not available when connected via SE20)

* X14: pulse disable, indicates whether the pulses for the thyristors are disabled or enabled

* X15: summated pulses (also at X5, Pin 9), this signal shows the firing pulses, with respect to time, as a function of the torque direction.
  In addition the firing pulses are modulated by the chopping frequency of the first and second pulses of the thyristor 1 . The oscillogram of both torque directions MI and MII is then as follows:



The X5 connector is designed for the supply of external signals and reading measurement signals during commissioning:

* external synchronization voltage

* external pulse disable

* synchronization of the pulse chain in conjunction with other PG's

* analog current actual value as from X12

* summated pulses as from X15

* synchronization voltage, digital after internal smoothing

* excitation current setpoint

3. Board Design

* connection for the local bus

* design for unforced ventilation

* CPU 80C186 - 16 MHz

* RAM 64 K Byte
  Battery backup from the power supply

* connector recess for the program memory module MS3,MS31,MS4,MS41,MS45

* 1 serial interface
  optional V 24, 20 mA (TTY)

* 4 binary inputs, non voltage isolated, interrupt controller, 24 V

* 4 binary outputs, non voltage isolated, 24 V, 50mA

* real time clock
  resolution 10 MS; Battery backup from the power supply

* 7 segment display for the configured processor number or error code

* board ID

* hardware and software monitoring by watchdogs

* test connectors for logic analyzers or recorders

* 50 pin SITOR interface with analog output for the excitation
  current control, 12 bit, 0-10V, 20mA

4. Application Notes

The processor board PG16 can be installed in both the wide rack (SR1, SR5) and the narrow rack (SR2, SR4). It requires two rack slots.

!! The board must never be inserted nor pulled when under power !!

An interface thick film circuit (hybrid module) must be installed to implement the Hex monitor dialog via the serial interface X01 .

* SS1: 20 mA (TTY) for PG 675/685

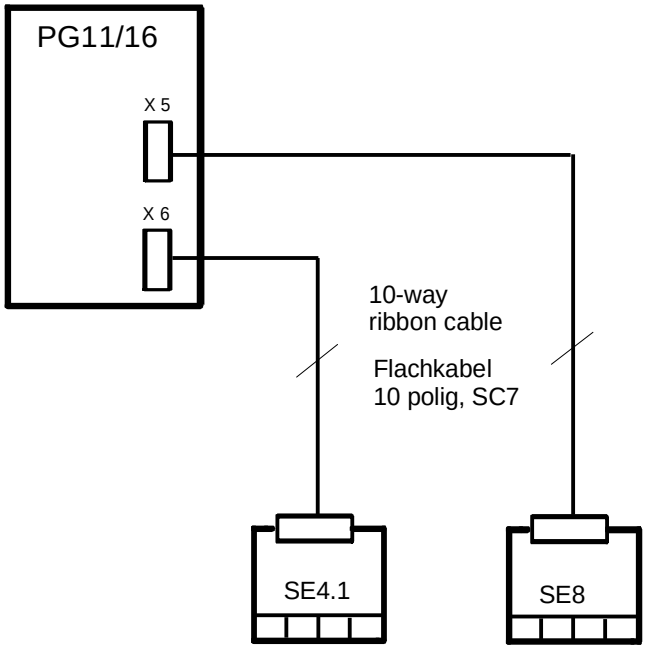
* SS2: V.24 (RS 232) for Televideo

The hybrid module must be installed on the X51 location for the X01 serial interface.

WARNING: CORRECT INSTALLATION IMPORTANT !

For commissioning it is recommended to connect the X5 connector with an interface module SE8, all necessary measuring signals are available here. Further information for commissioning see /2/.

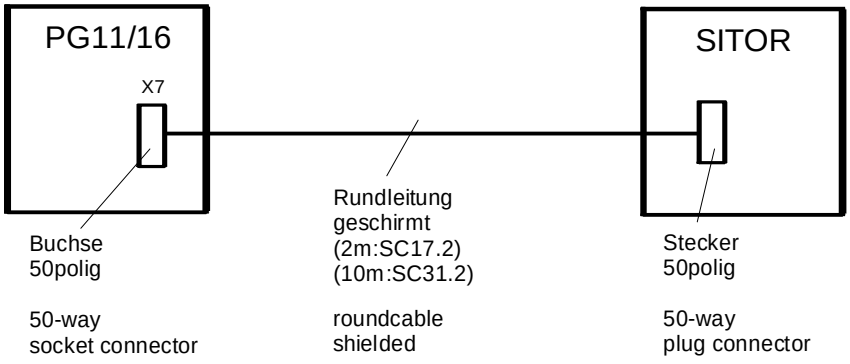
The binary inputs and outputs are connected to the interface module SE4.1 or SE8 (SE4.1 with an additional LED status display) from the X6 connector via a 10 pin ribbon cable. The external connections to the plant are also located there.



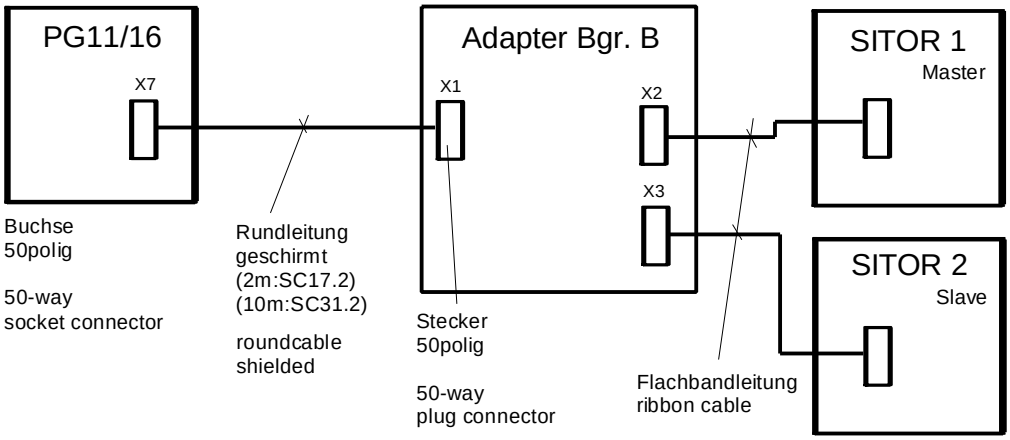
EXTERNEANSCHLÜßE

The SITOR set is connected to the X7 socket via a 50 pin cable. The following possibilities are available:

a) Connect the SITOR set directly to the PG16

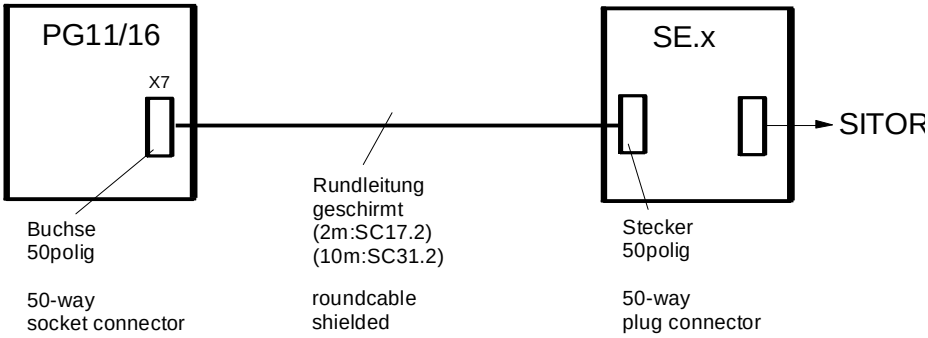


b) Connection of several SITOR sets in parallel via the adapter board B (take maximum output current of the pulse driver into consideration):



The exact connection setup may be taken from the corresponding handling instructions.

c) Connection to the interface module SE20...:



The SITOR interface is simulated in the interface board SE20 . This is required when connecting a SITOR cubicle system which does not have it's own interface. The output of the current actual value, in analog form, to the test jack X13 and X5 pin 6 is then no longer required.

The pins 3 (15V) and 4 on the X5 plug connector must be jumpered with a shorting bridge or switch in order to enable the thyristor firing pulses. This may be implemented either directly on the X5 plug or through a binary output (24V) of a connected interface module. A daisy chain bridge can be used to jumper the pins 3 and 4 on X5. Supplying 24V always requires an additional terminal block.

The synchronization voltage supply may be selected either from an external source via the X5 connector or an internal source from the SITOR set (X7). The default setting is the supply via X7 . The selection between X7 and X5 is implemented per software in the versions starting from V3.0 at the connector SYX in the function block TG6. Older software versions permit switching to X5 by removing the resistor R603.

The SITOR interface has 12 pulse output ports. The supply voltage is 24V DC, +25% / -20% . The output current for chain pulses [T(E)/T(P)=1:1] may reach the following maximum values:

* 150 mA for a pulse duration of 2 x 60 Grad (el.)
  for the phase power controllers

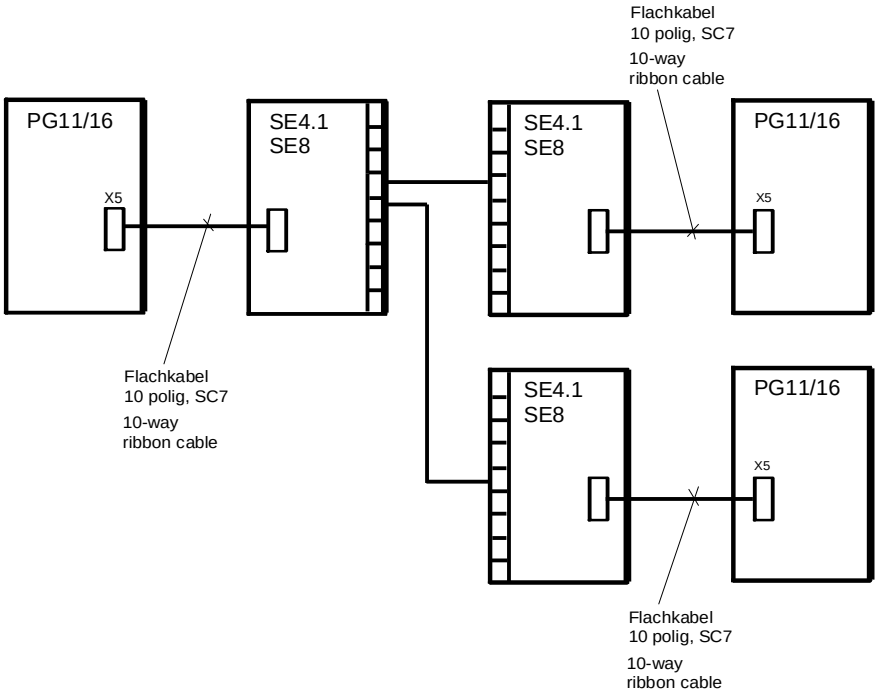
* 300 mA for a pulse duration of 2 x 30 Grad (el.)
  for cyclo-converters

* 300 mA for a pulse duration of 2 x 15 Grad (el.)
  for other converter circuits

Continuous pulses can also be generated instead of the chain pulses (7.8 Khz modulation). The selection between is implemented per software in the versions starting from V3.0 at the connector LDP in the function block TG6. Older software versions permit switching to long pulses by removing the resistor R601. The pulse modulation is therefore disabled, the maximum output current is halved. Remove the resistor R605 when an application requires the secondary pulses to be completely disabled.

The output X5/5 is for pulse synchronization when several processor boards PG16 or current converters (i.e. cyclo-converters) are used. A PG16 sets the time point for the firing pulse such that several thyristors in a series connection are all triggered simultaneously.

The connection of individual PG16 boards is as follows:



Electrical data of the synchronization output:

* Output voltage 'H' approx. 14 V

* maximum output current 'H' approx. 40 mA

* maximum delay 1 us

* Adapter board B 6QX 5318

5. Technical Specification

General Data

INSULATION GROUP	A to VDE 0110 (power side) paragraph 13, group 2 at 24 VDC, 15VDC, 5 VDC
AMBIENT TEMPERATURE	0 to 55 deg. C
STORAGE TEMPERATURE	-40 to +70 deg. C
HUMIDITY CLASS	F to DIN 40040
ALTITUDE RATING	S to DIN 40040
MECHANICAL STRESS	Installation in fixed vibration resistant devices
PACKAGING SYSTEM	ES 902 C
DIMENSIONS	233.4 x 220 mm
BOARD WIDTH	2 2/3 SEP = 2 Slot = 40.28 mm
WEIGHT	0.7 kg
CURRENT CONSUMPTION	5 VDC 2.3 A with MS31 +15 VDC 50mA -15 VDC 50mA Vbatt 10 uA in backup operation

BINARY INPUTS

NUMBER	4 not voltage isolated
INPUT VOLTAGE	+24 V Rated value
INPUT VOLTAGE	
FOR 0 SIGNAL	-1 V to +6 V; or Binary inputs open
FOR 1 SIGNAL	+13 V to +33 V
INPUT CURRENT	
AT 1 SIGNAL	Typ. 3 mA
DELAY TIME	200 uS (Input filter)

BINARY OUTPUTS

NUMBER	4 not voltage isolated
SUPPLY VOLTAGE	
-RATED VALUE	24 VDC-
-HARMONICS	3.6 VDC
-PERM. RANGE	+ 20 to + 30 V incl. harmonics
-TRANSIENTS	+ 35 V smaller than 0,5 sec.
OUTPUT CURRENT AT 1 SIGNAL	
-RATED VALUE	50 mA
SHORT CIRCUIT PROTECT.	electronic
INDUCTIVE LIMIT	
TRIPPING VOLTAGE	to Up + 1V
RESIDUAL CURRENT	20 uA at 0 Signal
SIGNAL LEVEL	
-AT 0 SIGNAL	max. 3V
-AT 1 SIGNAL	min. supply - 2,5V
Switching delay	15 uS

EXTERNAL SYNCHRONIZATION VOLTAGE

- RATED VALUE	15 V eff.
- PERM. RANGE	10 to 20 V eff.
- LOADING	20 kOhm input impedance, Differential input

ANALOG OUTPUT

- RANGE	0 - 10 V
- ACCURACY	10 bit
- RESOLUTION	12 bit

- OUTPUT CURRENT 20 mA protected against short circuit

6. Pin Allocation of the PG16

6.1. Pin Allocation of the Serial Interface X01

PIN	V 24		20 mA (TTY)	
1	FRAME GROUND		FRAME GROUND	
2	TRANSMIT DATA OUT	T*D	---	
3	RECEIVE DATA IN	R*D	---	
4	REQUEST TO SEND OUT	*RTS	---	
5	CLEAR TO SEND	*CTS	---	
6	DATA SET READY IN		---	
7	GROUND		---	
8	DATA CARRIER DETECT IN	*DCD	---	
9	GROUND		GROUND	
10	---		CURRENT LOOP + TRANSMIT	+T*D
11	+15 V		+15 V	
12	---		20 MA SOURCE 1	
13	---		CURRENT LOOP + RECEIVE	+R*D
14	---		CURRENT LOOP - RECEIVE	-R*D
15	RECEIVE/TRANSMIT CLOCK	*RT*C	---	
16	---		20 MA SOURCE 2	
17	RECEIVE/TRANSMIT CLOCK		---	
18	GROUND		GROUND	
19	---		CURRENT LOOP - TRANSMIT	-T*D
20	DATA TERMINAL READY OUT		---	
21	---		20 MA DRAIN 2	
22	+5 V		+5 V	
23	+5 V		+5 V	
24	TRANSMIT RECEIVE CLOCK	*TR*C	20 MA DRAIN 1	
25	-15 V		-15 V	

6.2. Pin Allocation of the External Signals X5

Pin	Designation
1	External synchronization voltage
2	Reference voltage to pin 1
3	P15 Output, 15 V
4	External pulse disable connected via switch to pin 3 jumpered = pulses enabled open = pulses disabled
5	Synchronization of the pulse chains, connected with further PG16's Output voltage 'H' approx. 14 V Output current, max. 'H' 40 mA
6	Analog current actual value ±10 V, Ri = 2.2kOhm
7	Excitation current setpoint 0..10V, Ri = 2.2kOhm
8	Ground (digital), reference voltage
9	Summated pulses as in X 15
10	Display zero indication of synchronization voltage Logic level 15 V, Ri = 2,2kOhm for H-Signal