3.2 K4LCN-X Node Processor

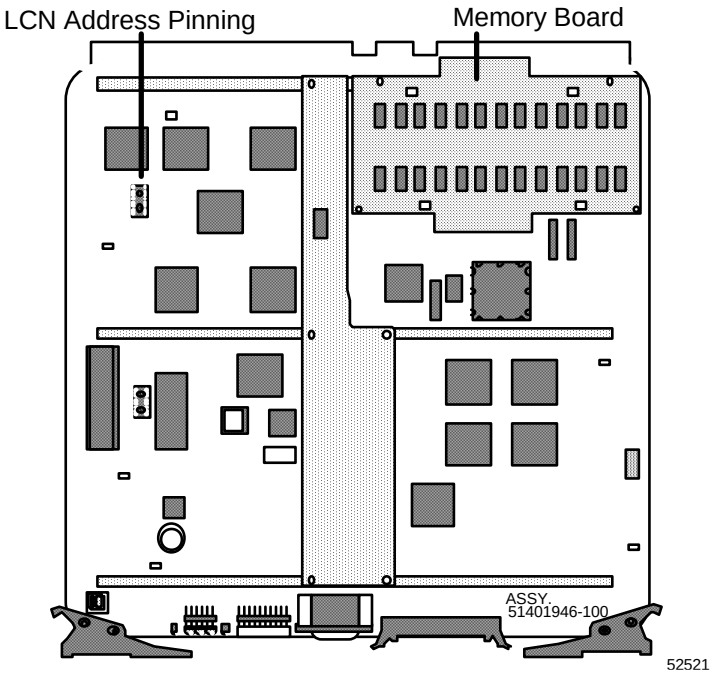
Overview

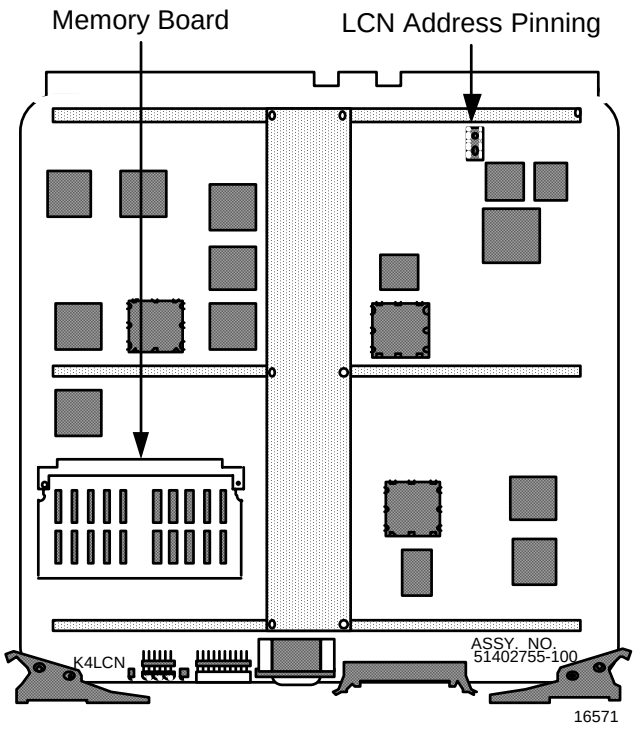
The K4LCN processor board contains all of the essential parts to make up the kernel portion of any LCN node. It includes a 68040 processor, LCN interface circuits, and 8 or 16 megawords of on-board memory (for the A^XM). It has floating point calculation hardware capability. The exact memory size is determined by which memory option is purchased. A minimum of 6 megawords is required to support the A^XM with R500 software.

Changing memory size requires the replacement of the existing memory daughter board or mezzanine board with a board that contains the proper memory complement. The memory board can be upgraded in the field.

The K4LCN board memory size is easily recognized by the -X portion of the name on the left extraction lever. (K4LCN-8 = 8 megawords, K4LCN-16 = 16 megawords).

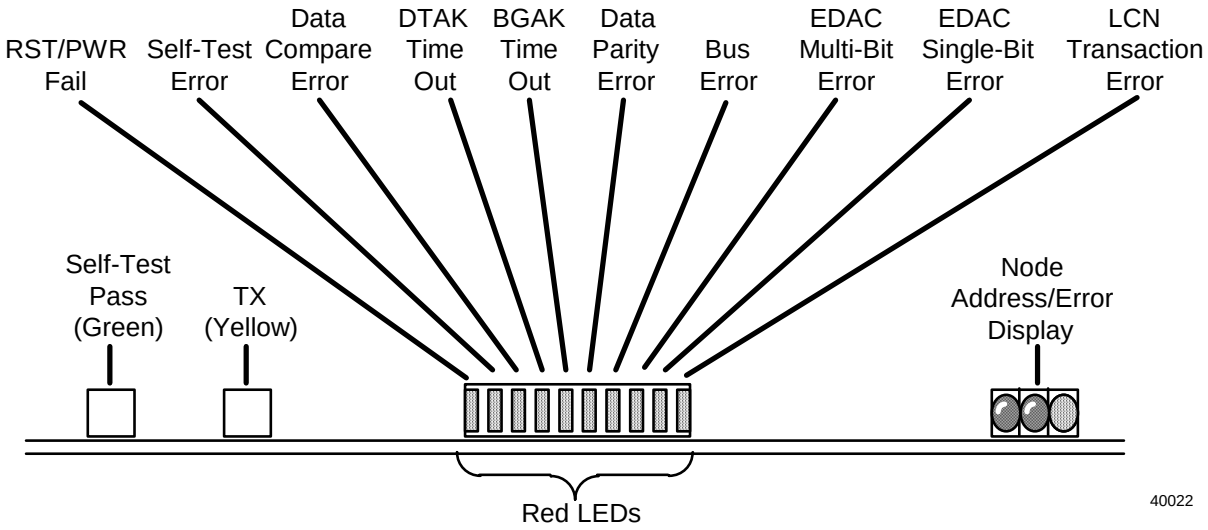
The following board assembly layout illstrations show a top view of the early production K4LCN board, assembly 51401946-100, and the latest production K4LCN board, assembly 51402755-100.




Memory Board
LCN Address Pinning
K4LCN
ASSY. NO.
51402755-100
16571

K4LCN indicators

The K4LCN board indicators are visible at the free edge of the board while it is installed in the module chassis. They provide visual indication of the existing conditions of the board. See the illustration below.



Indicator description

The following table provides a description of the indicators on the K4LCN board. Reference the preceding diagram.

Table 3-2 K4LCN Board Indicators

LED	Description	Suspected cause if abnormal
Self-Test Pass	On after board passes self-test. Normally on.	K4LCN
TX	On when transmitting on the LCN. Normally on or flashing rapidly.	K4LCN
RST/PWR fail	On when a reset operation caused by the reset button or power on is in progress. Normally off.	K4LCN
Self-Test Error	On to indicate a board self-test error. Normally off.	K4LCN
Data Compare Error	On to indicate an on-board data compare error. Normally off.	K4LCN
DTAK Time Out	On to indicate a Data Transfer Acknowledge failure. Normally off.	K4LCN
BGAK Time Out	On to indicate a Bus Grant Acknowledge failure. Normally off.	K4LCN or other board(s) in chassis
Data Parity Error	On to indicate an on-board data parity error. Normally off.	K4LCN
Bus Error	On to indicate a detected backplane bus parity error. Normally off.	K4LCN, other board(s) in chassis, or backplane
EDAC Single-Bit Error	On to indicate a single-bit (correctable) RAM error. Normally off.	K4LCN
EDAC Multiple-Bit Error	On to indicate a multiple-bit (uncorrectable) RAM error. Normally off.	K4LCN
LCN Transaction Error	On to indicate communication problems with the LCN. Normally off.	K4LCN or CLCN A/B I/O (LCN I/O) or LCN network
Node Address/Error display	This 3-digit display normally displays the pinned LCN node address. It will display error codes for further problem definition in error situations.	See *Five/Ten-Slot Module Service* manual for multiple possible causes. Reference >>Alpha Numeric Displays in Appendix A.

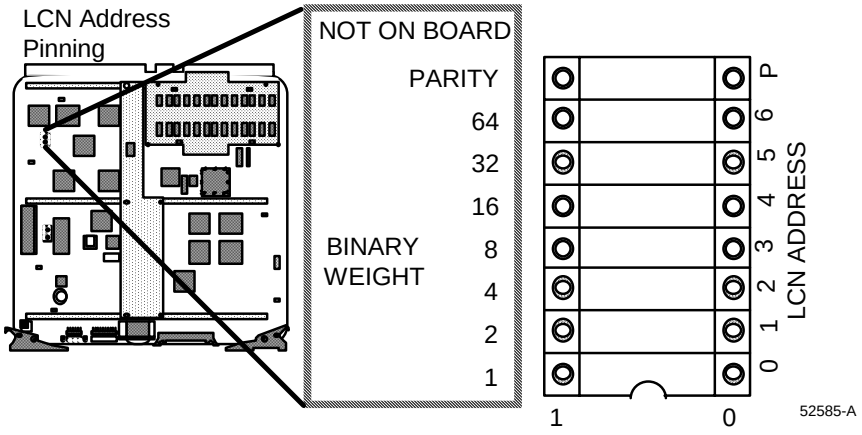
K4LCN Pinning

The K4LCN board has an LCN node number pinning feature on the board itself. This feature is duplicated on the CLCN A/B I/O or LCN I/O board that is installed directly behind the K4LCN board in the AXM Five-Slot Module chassis.

ATTENTION

The address pinning jumpers must all be removed from the K4LCN board when it is used in conjunction with a CLCN A/B I/O (or LCN I/O) board. The node number pinning must be done on the CLCN A/B I/O (or LCN I/O) board in this case.

The following illustration shows the LCN address pinning for a K4LCN board when used in the A^{X}M's Five-Slot Module chassis.The illustration shows the location of the pinning block, TS2, on the early production K4LCN board, assembly 51401946-100.



The pinning requirements are the same for the latest production K4LCN board, assembly 51402755-100. Refer to the previous illustration of the board's assembly layout for the approximate location of the pinning block, TS1.

K4LCN Memory

Memory for the K4LCN board is provided by a vertically pluggable daughter board on the early production K4LCN board, assembly 51401946-100, and a horizontally pluggable DIMM (Dual Iline Memory Module) style mezzanine board on the latest production K4LCN board, assembly 51402755-100.

The memory daughter board is also sometimes referred to as a mezzanine board.

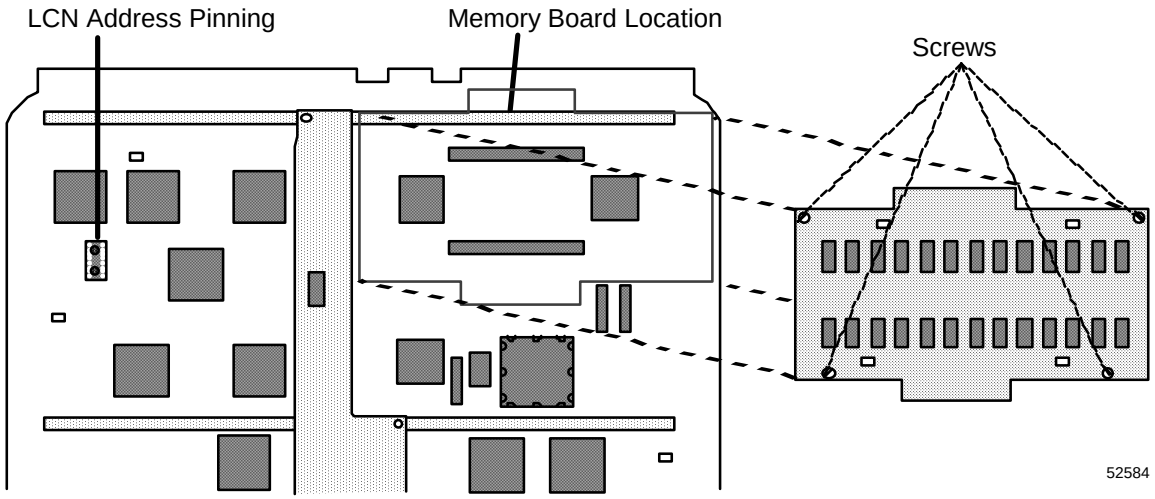
The memory boards are available in three memory sizes, 4, 8, and 16 megawords.

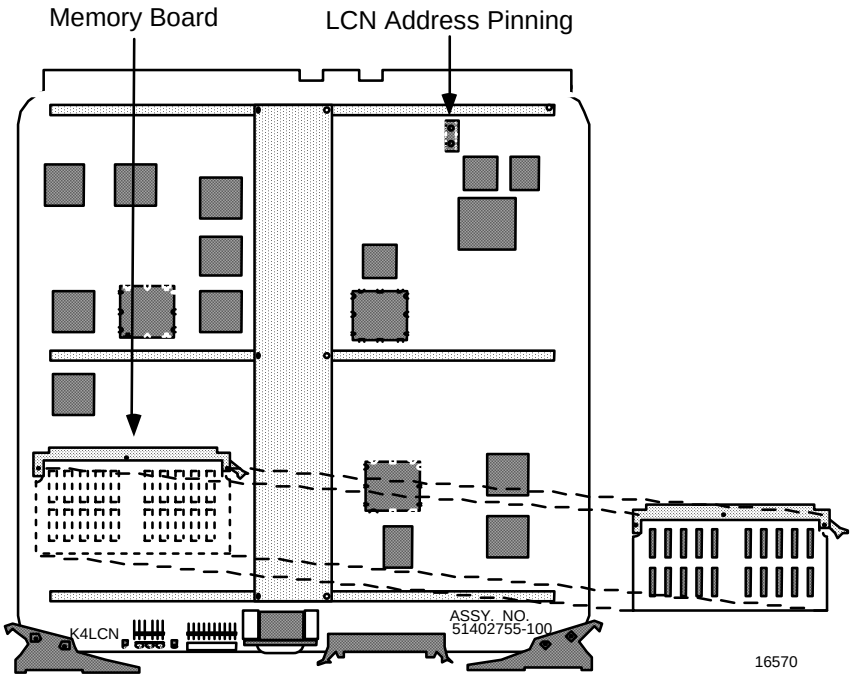
When a replacement K4LCN board is ordered from Honeywell logistics, it is provided without a memory board. The appropriate size memory board should also be ordered separately to prevent the possibility of moving a defective memory board from the failed K4LCN board to the replacement board.

The size of the memory on the K4LCN board is upgraded in the field by replacing the memory board.

Earlier memory boards, such as EMEM, PMEM, or QMEM, that were used with earlier node processor boards cannot be used with the K4LCN board.

The following illustrations show the installation of the memory boards on the early and latest production K4LCN boards.




Memory Board
LCN Address Pinning
K4LCN
ASSY. NO.
51402755-100
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