COPROCESSOR REGISTER MAP

The MVME133A responds to only two types of CPU space accesses (FC2 – FC0 = 111): coprocessor and interrupt acknowledge. The function code space decoder selects the MC68881 anytime the MPU executes a coprocessor cycle (FC2 – FC0 = 111 and A19 – A16 = 0010). The recommended coprocessor ID (bits 9-11 of the coprocessor instruction word) for the MC68881 is 001. However, the MVME133A selects the MC68881 regardless of the ID. The MC68881 registers are addressed by A04-A01 as shown in Table 3.

Table 3. Coprocessor Register Map

A04–A00 (In Binary)	MC68881 Register D31 – D16		MC68881 Register D15 – D00	
00000	Response	(Read Only)	Control	(Write Only)
00100	Save	(Read Only)	Restore	(Read/Write)
01000	Reserved		Command	(Write Only)
01100	Reserved		Condition	(Write Only)
10000	Operand		(Read/Write)	
10100	Register Select (Read Only)		Reserved	
11000	Instruction Address		(Write)	
11100	Operand Address		(Read/Write)	

INTERRUPT HANDLER AND INTERRUPT ACKNOWLEDGE MAP

The interrupt handler gives the onboard MPU the ability to sense and respond to all onboard interrupts, all seven VMEbus interrupts, VMEbus ACFAIL*, VMEbus SYSFAIL* and the ABORT switch. All of the VMEbus interrupts and the ABORT interrupt can be enabled/disabled by jumpers. All other interrupts are enabled/disabled individually under software control. Also all interrupts may be disabled with a software control bit.

Function code space decoder selects the interrupt handler anytime the MC68020 executes an Interrupt Acknowledge cycle (FC2 – FC0 = 111 and A19 – A16 = 1111). The interrupt handler then determines the acknowledge level by examining A01-A03. It then decides which device the interrupt acknowledge cycle is for. If the acknowledge cycle was for VMEbus ACFAIL*, ABORT switch or real-time clock, the interrupt handler causes the MC68020 to generate the interrupt vector internally. If not, the interrupt handler initiates a vector fetch cycle for the appropriate device. If both onboard and VMEbus interrupts are activated on the same interrupt level, the interrupt handler will acknowledge the onboard interrupt first.

Table 4 summarizes all the interrupt sources and their associated interrupt vectors.

Table 4. Interrupt Sources and Vectors

Interrupt Source	Path	Vector Passed	Vector Offset	Level
VMEbus IRQ1*	Direct	From Interrupting VMEbus Slave	4 x Vector	1
VMEbus IRQ2*	Direct	Same As Above	4 x Vector	2
VMEbus IRQ3*	Direct	Same As Above	4 x Vector	3
VMEbus IRQ4*	Direct	Same As Above	4 x Vector	4
MM58274A Real-Time Clock	Direct	None	$70	4
VMEbus IRQ5*	Direct	From Interrupting VMEbus Slave	4 x Vector	5
DDTR*	MC68901 GPIO0	Refer to MC68901 Data Sheet	4 x Vector	5
VMEbus BERR*	MC68901 GPIO1	Refer to MC68901 Data Sheet	4 x Vector	5
LTO Local Bus Timeout	MC68901 GPIO2	Refer to MC68901 Data Sheet	4 x Vector	5
MC68901 Timer D	MC68901	Refer to MC68901 Data Sheet	4 x Vector	5
MC68901 Timer C	MC68901	Refer to MC68901 Data Sheet	4 x Vector	5

(continued)

Table 4. Interrupt Sources and Vectors (continued)

Interrupt Source	Path	Vector Passed	Vector Offset	Level
MC68901 Timer B	MC68901	Refer to MC68901 Data Sheet	4 x Vector	5
Transmit Error (Serial)	MC68901	Refer to MC68901 Data Sheet	4 x Vector	5
Transmit Buffer Empty (Serial)	MC68901	Refer to MC68901 Data Sheet	4 x Vector	5
Receive Error (Serial)	MC68901	Refer to MC68901 Data Sheet	4 x Vector	5
Receive Buffer Full (Serial)	MC68901	Refer to MC68901 Data Sheet	4 x Vector	5
MC68901 Timer A	MC68901	Refer to MC68901 Data Sheet	4 x Vector	5
OIRQ (Bus Interrupter)	MC68901 GPIO6	Refer to MC68901 Data Sheet	4 x Vector	5
VMEbus SYSFAIL	MC68901 GPIO7	Refer to MC68901 Data Sheet	4 x Vector	5
VMEbus IRQ6*	Direct	From Interrupting VMEbus Slave	4 x Vector	6
Z8530 Serial Ports	Direct	Refer to Z8530 Data Sheet	4 x Vector	6
VMEbus IRQ7*	Direct	From Interrupting VMEbus Slave	4 x Vector	7
VMEbus ACFAIL	Direct	None	$7C	7
ABORT*	Direct	None	$7C	7

MULTIFUNCTION PERIPHERAL

The MVME133A uses the multifunction peripheral (MC68901) for its front panel debug port, tick timers, watchdog timer and the status and control registers. The MC68901 has the ability to interrupt the MPU on level 5 when required for the timers, debug port and GPIO (status) bits.

MC68901 DEBUG PORT

The front panel debug port is a minimal implementation of an RS-232-C serial port. It uses RXD as its transmit data output and TXD as its receive data input. DSR is driven true and DCD is pulled up to +12 V. CTS is controlled by a software bit and RTS is monitored by another software bit, providing minimal flow control.

The baud rate generator for the serial port is timer C in the MC68901. The XTAL input to the MC68901 is 1.23 MHz, supporting baud rates from 110-9600 baud.

MC68901 TIMERS

There are four timers in the MC68901. They are assigned as follows:

Timer A — Software tick timer.
Timer B — Tick timer overflow/watchdog timeout.
Timer C — Baud rate generator for the front panel serial debug port.
Timer D — Delay mode only. Unassigned.

NOTE: The watchdog timeout resets the MPU module when the timer B output is high.

MC68901 GENERAL PURPOSE I/O

The MC68901 has eight General Purpose I/O pins. The MVME133A uses five of these pins as status inputs and three of them as control outputs. The assignment of GPIO0-GPIO7 is shown in Table 5.

MODULE STATUS REGISTER

In addition to the general purpose status and control bits of the MC68901, the MVME133A has eight read only status bits. Collectively, these bits are called the module status register (MSR). The MSR and the MC68901 are grouped together and appear as a 16-bit word port to the MPU. Therefore, it is important to note that even though the MSR ignores all write accesses, a write to the MSR will affect the MC68901.

The bit assignments for the module status register are shown in Table 6.

Z8530 DUAL SERIAL PORTS

The MVME133A uses the Z8530 to implement its two multiprotocol serial ports, providing multifunction support for handling the large variety of serial communications protocols available. The Z8530 can be programmed to satisfy special serial communications requirements as well as to follow standard formats such as byte-oriented synchronous, bit-oriented synchronous and asynchronous. In addition, protocol variations are supported within each operating mode by checking odd or even parity, character insertion or deletion, CRC generation and checking, break and abort generation and detection and many other protocol dependent features.

Table 5. GPIO Register

GPIO7 INPUT	GPIO6 INPUT	GPIO5 OUTPUT	GPIO4 OUTPUT	GPIO3 OUTPUT	GPIO2 INPUT	GPIO1 INPUT	GPIO0 INPUT

GPIO7 — VMEbus SYSFAIL Flag
GPIO6 — VMEbus IRQ3 Request Flag
GPIO5 — Board or System Failure Control
GPIO4 — Enable/Disable Interrupts Control
GPIO3 — DCTS Control
GPIO2 — Local Bus Timeout Flag
GPIO1 — VMEbus BERR Flag
GPIO0 — DRTS Flag

Table 6. Module Status Register

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT09	BIT08
ACFAIL	SYSCON	PWRUP*	SRBIT4	SRBIT3	SRBIT2	SRBIT1	SRBIT0

ACFAIL — VMEbus AC Power Fail
SYSCON — VMEbus System Controller
PWRUP* — Power-Up Reset
SRBIT4 — Status Register Bit 4
SRBIT3 — Status Register Bit 3
SRBIT2 — Status Register Bit 2
SRBIT1 — Status Register Bit 1
SRBIT0 — Status Register Bit 0

Because of the internal structure of the Z8530, there are several means of obtaining the baud rate clocks for each of the two serial channels. Many of the more frequently used baud rates are supported by the MVME133A internally, with additional support provided for external generation of any other desired frequency. Reference should be made to the Z8530 Data Manual and the MVME133A User's Manual for additional information.

All drivers and receivers for both serial channels are provided on the MVME133A, with port A implemented for RS-485/RS-422 and port B for RS-232 communications. User can configure the RS-232-C port (Port B) as DCE or as DTE using the jumpers provided by MVME133A. The RS-485 port may be configured by software to be Master or Slave, full duplex or half duplex. All signals are made available on rows A and C of the VMEbus P2 connector. The RS-232 connections can be made directly from P2 to a DB-25 connector, although the RS-485 may require a crossover cable. Refer to the MVME133A User's Manual for pinout information.

REAL-TIME CLOCK

The Real-Time clock on the MVME133A is an MM58274, providing a timekeeping function from tenths of seconds to tens of years in independently accessible registers, an hours counter programmable for 12- or 24-hour operation, an independent interrupting timer and its own onboard crystal controller oscillator. The counters are arranged as 4-bit words and can be randomly accessed for reading and setting time.

ONBOARD ROM/PROM/EPROM/EEPROM

The MVME133A has four 28-pin ROM/PROM/EPROM/EEPROM sockets that are organized as two banks with two sockets per bank. Each bank appears as a 16-bit word port to the MPU and can be separately configured for 8Kx8, 16Kx8, 32Kx8 or 64Kx8 ROM/PROM/EPROMs or for 2Kx8, 8Kx8 or 32Kx8 EEPROMs. When a bank is configured for EEPROM, writes to that bank must always be 16-bits wide.

There are several different algorithms for erasing/writing to EEPROMs, depending on the manufacturer. The MVME133A supports only those devices which have a "Static RAM" compatible erase/write mechanism. Note that the MVME133A requires that the EEPROMs allow wired-OR on the RDY/BSY* pin.

VMEbus INTERFACE

The MVME133A provides an A32/D32 VMEbus interface for buffering of data, address and control, for word data manipulation to accommodate MC68020 and VMEbus data handling differences and for interrupt handling and control of misaligned transfers. In addition, system controller functions are available including a VMEbus time-out generator, a SYSCLK driver, an IACK* daisy-chain driver, a SYSRESET* driver and a level three arbiter. All of these system controller functions are enabled/disabled by a jumper on the MVME133A.

VMEbus REQUESTER

The VMEbus requester is used to obtain and relinquish mastership of the VMEbus. The MVME133A operates in the Early Release-on-Request (ROR) mode and can request VMEbus mastership on any one of the four request levels, depending upon jumper configurations on the MVME133A.

VMEbus INTERRUPTER

The MVME133A's single-level Interrupter generates interrupt requests on IRQ3*. It provides the value $FF as its status ID byte. It is an 8-bit interrupter and responds to all sizes of interrupt acknowledge cycles. The interrupter drives IRQ3* whenever the MPU performs a read access to a location within FFFB8000 to FFFBFFFF. The state of the interrupter is reflected as the OIRQ (GPIO6) bit of the MFP GPIO port.

Table 7. MVME133A Timing
(All Times Are Total Cycles)

Access Sequence	MVME133A		Notes
	Read	Write	
MPU to local DRAM	4 Cycles	4 Cycles	1, 2
MPU to local ROM/ PROM/EPROM/EEPROM	6 Cycles	6 Cycles	1, 3
VMEbus to local DRAM	9 Cycles (450 ns)	9 Cycles (450 ns)	4, 5
MPU to global RAM (MVME133A)	13 Cycles	14 Cycles	5, 6
MPU to global RAM (MVME204-1)	9 Cycles	7 Cycles	6, 7

NOTES: 1. No arbitration overhead.
2. Except RMW cycles where MVME133A is required to obtain VMEbus mastership before RAM cycle can be started.
3. Device access time must be 200 ns or less.
4. DS0*/DS1* asserted to DTACK* time.
5. Typical values. Actual values may be greater or less depending on the state of the slave MVME133A.
6. Assume the master MVME133A is the current VMEbus master.
7. The total number of clock cycles = 4 + (Ta/T) for a READ and 5 + (Ta/T) for a WRITE, where Ta = DS0*/DS1* to DTACK* time, and T = MPU clock period.

MECHANICAL AND ENVIRONMENTAL SPECIFICATIONS

Characteristics	Specifications
Power Requirements MVME133A-20	+5 Vdc, 7 A max, 5 A typ ±12 Vdc, 250 mA max
Clock Frequency MVME133A-20	20.0 MHz clock frequency
Operating Temperature	0° to 55°C Inlet air temperature with forced air cooling
Storage Temperature	−40° to 85°C
Relative Humidity	5% to 90% (non-condensing)
Physical Dimensions Height Width	10.31 in (261.8 mm) 7.40 in (188.0 mm)
Thickness	0.83 in (21.0 mm)

ORDERING INFORMATION

Part Number	Description
MVME133A-20	VMEmodule 32-bit Monoboard Microcomputer with 20.0 MHz MC68020 CPU. Includes User's Manual.
MVME133A/D	VMEmodule 32-Bit Monoboard Microcomputer User's Manual.

RELATED PRODUCTS

Part Number	Description
MVME133Abug	MVME133Abug Diagnostic/Debug Package for the MVME133A. Includes User's Manual.
MVME225	VMEmodule 2Mb Dynamic RAM with Byte Parity. Includes User's Manual.
MVME215-1/-2/-3	256Kb/512Kb/1Mb CMOS RAM Module. Includes User's Manual.
M68V2XSBG133	MVME133Abug Source and Object Modules on 5¼'' Diskette. Includes User's Manual.