Preface

This document provides general board level hardware description, hardware preparation and installation instructions, as well as debugger general information and instructions for the MVME172LX VME Embedded Controller (which is available in the versions listed below).

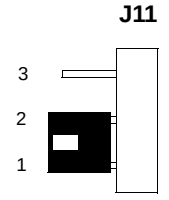
Assembly Item	Board Description
MVME172-213	4MB DRAM, 64 MHz MC68LC060, SCSI & Ethernet Interface
MVME172-223	4MB DRAM, 60 MHz MC68060, SCSI & Ethernet Interface
MVME172-233	4MB ECC DRAM, 64 MHz MC68LC060, SCSI & Ethernet Interface
MVME172-243	4MB ECC DRAM, 60 MHz MC68060, SCSI & Ethernet Interface
MVME172-253	16MB ECC DRAM, 64 MHz MC68LC060, SCSI & Ethernet Interface
MVME172-263	16MB ECC DRAM, 60 MHz MC68060, SCSI & Ethernet Interface
MVME172-303	8MB DRAM, 64 MHz MC68LC060, SCSI & Ethernet Interface
MVME172-313	8MB DRAM, 60 MHz MC68060, SCSI & Ethernet Interface
MVME172-323	8MB ECC DRAM, 64 MHz MC68LC060, SCSI & Ethernet Interface
MVME172-333	8MB ECC DRAM, 60 MHz MC68060, SCSI & Ethernet Interface
MVME172-343	32MB ECC DRAM, 64 MHz MC68LC060, SCSI & Ethernet Interface
MVME172-353	32MB ECC DRAM, 60 MHz MC68060, SCSI & Ethernet Interface
MVME172-363	16MB DRAM, 64 MHz MC68LC060, SCSI & Ethernet Interface
MVME172-373	16MB DRAM, 60 MHz MC68060, SCSI & Ethernet Interface

The MVME172LX VME Embedded Controller will be referred to as “MVME172LX” throughout this document.

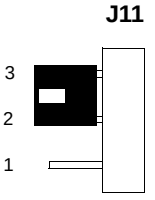
This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system, or work in a lab environment for experimental purposes. A basic knowledge of computers and digital logic is assumed. Companion publications are listed in Appendix E.

Caution

The setting of the IP32 CSR bit (IP2 chip, register at offset $1D, bit 0) must correspond to that of the jumper. The bit is cleared (0) for 8MHz, or set (1) for 30/32MHz. If the jumper and the CSR bit are not configured the same, the board may not run properly.



8MHz IP Bus Clock
(Factory configuration)



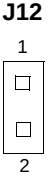
30/32MHz IP Bus Clock
(from MPU Bus Clock)

SCSI Terminator Enable Header (J12)

The MVME172LX provides terminators for the SCSI bus. The SCSI terminators are enabled/disabled by a jumper on header J12. The SCSI terminators may be configured as follows:



Onboard SCSI Bus Terminator Enabled
(Factory Configuration)



Onboard SCSI Bus Terminator Disabled

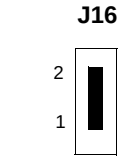
Note If the MVME172LX is to be used at one end of the SCSI bus, the SCSI bus terminators must be enabled.

Thermal Sensing (J13)

J13 is a two-pin header to access the M68060 THERM1 and THERM0 pins. These pins are connected to an internal thermal resistor that can be used to provide information about the average temperature of the die. J13 is not configurable.

Flash Write Protect Header (J16)

When the Flash write protect jumper is installed (factory configuration), the Flash memory can be written to via the normal software routines. When the jumper is removed, Flash memory cannot be written.



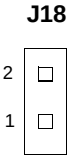
Flash Write Protect
(Factory configuration)

IP Bus Strobe Select Header (J18)

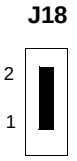
Some IP bus implementations make use of the Strobe∗ signal (pin 46) as an input to the IP modules from the IP2 chip. Other IP interfaces require that the strobe be disconnected.

With a jumper installed between J18 pins 1 and 2, a programmable frequency source is connected to the Strobe∗ signal on the IP bus. Refer to the IP2 chip programming section in the *MVME172 Embedded Controller Programmer's Reference Guide* for additional information.

If the jumper is removed from J18, the strobe line is available for a sideband type of messaging between IP modules. The Strobe∗ signal is not connected to any active devices on the board, but it may be connected to a pull-up resistor.

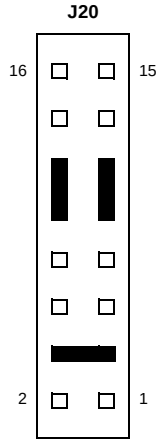


IP Strobe disconnected
(Factory configuration)

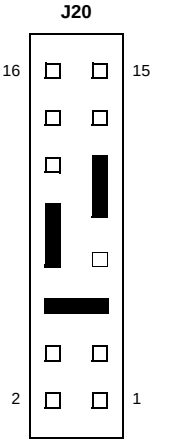


IP Strobe connected

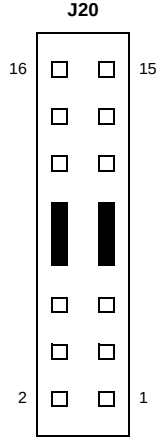
J20 supplies eight jumper headers for configuration of the EPROM sockets.



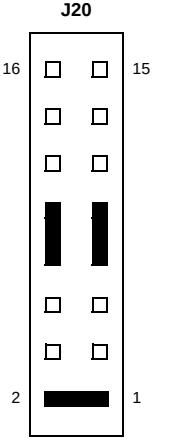
CONFIGURATION 1: 256K x 8 EPROMs



CONFIGURATION 2: 512K x 8 EPROMs (default)



CONFIGURATION 3: 1M x 8 EPROMs



CONFIGURATION 4: 1M x 8 EPROMs
ONBOARD FLASH DISABLED

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