

JEPMC-CP200

CPU Controller Module

YASKAWA JEPMC-CP200 is the CPU-01 processor module for the MP920 Machine Controller. It provides 2 MB flash memory, 2 MB battery-backed SRAM and two configurable RS-232C communication ports.

IDENTITY	VERIFIED VALUE
Manufacturer	YASKAWA
Complete model	JEPMC-CP200
Product role	CPU Controller Module
System family	MP920 Machine Controller
Country of origin	Japan

DOCUMENT SCOPE

Exact identity, verified technical data, installation checks, applications, precautions and controlled acceptance records for this model.

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Technical Specifications

PARAMETER	VERIFIED VALUE
Model	JEPMC-CP200
Module designation	CPU-01
Controller family	MP920
Flash memory	2 MB
SRAM	2 MB, battery backed
Serial ports	Two RS-232C ports
Serial rates	9.6, 14.4 or 19.2 kbit/s
Connector	Female 9-pin D-sub
Supported serial modes	MEMOBUS, no-protocol and MELSEC
Current consumption	980 mA
Country of origin	Japan

System Role and Core Functions

YASKAWA JEPMC-CP200 is the CPU-01 processor module for the MP920 Machine Controller. It provides 2 MB flash memory, 2 MB battery-backed SRAM and two configurable RS-232C communication ports.

FUNCTION 1 MP920 CPU-01 processing module	FUNCTION 2 2 MB flash application memory
FUNCTION 3 2 MB battery-backed SRAM	FUNCTION 4 Two configurable RS-232C ports

Common Applications

APPLICATION	ENGINEERING CONTEXT
MP920 machine control	Executes the approved sequence and motion-related application in the MP920 controller.
Serial device integration	Uses the documented RS-232C ports for MEMOBUS, no-protocol or MELSEC communication.
Controller maintenance	Provides the exact CPU-01 identity for controlled replacement and restoration.
Legacy automation support	Maintains the documented MP920 hardware and memory architecture.

Engineering Precautions

- Verify the complete JEPMC-CP200 marking and CPU-01 designation.
- Back up the application, register data and communication parameters.
- Record rack position and every connected RS-232C cable.
- Check battery status before disturbing battery-backed SRAM.
- Remove controller power and use ESD controls before module handling.
- Preserve DIP-switch positions unless the Yaskawa procedure requires a change.
- Restore each serial port with the documented protocol and baud rate.
- Verify READY, RUN and diagnostic indications before release.

MODEL-SPECIFIC BOUNDARY

Back up the MP920 application, communication settings and memory records before replacement. Confirm the JEPMC-CP200 marking, rack position, battery condition and serial-port assignments, then verify controller status and communications before release.

Model-Specific FAQ

QUESTION	ANSWER
What is YASKAWA JEPMC-CP200?	It is the CPU-01 processor module for the MP920 Machine Controller.
How much flash memory is provided?	The Yaskawa manual specifies 2 MB of flash memory.
How much SRAM is provided?	The module has 2 MB of battery-backed SRAM.
How many serial ports are available?	Two RS-232C ports are provided on female 9-pin D-sub connectors.
Which serial rates are documented?	The manual lists 9.6, 14.4 and 19.2 kbit/s.
Which serial modes are supported?	The ports can be configured for MEMOBUS, no-protocol or MELSEC operation as documented.
Why must the battery be checked?	SRAM is battery backed, so battery condition affects retention of data when controller power is removed.
What confirms successful commissioning?	The controller enters the approved state, diagnostics are clear and both configured serial links pass their functional checks.

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